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Dual Coding Technique to Reduce Dynamic Power Dissipation and Delay in Network on Chip (NOC)

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Abstract— In a typical bus system of NOC, 10% of the power dissipation is static or leakage and 90% is dynamic power. Hence, Dynamic power dissipation reduction is main objective of our current research work. In our current research work power dissipation is reduced in deep submicron (DSM) technology. It has been found that 75% of dynamic power dissipation is due to coupling transitions whereas only 25% is due to self-transitions. This paper develops a novel technique, Dual Coding algorithm, in which inter-wire capacitance considers sufficiently and reduces the average power dissipation due to coupling transition approximately up to 66.66% for 8-bit and 16 bit wide data bus, 63.63% for 32-bit wide data bus, 56.66% for 64-bit wide data bus and delay by 13% - 13.63% for 8 bit, 16 bit, 32 bit and 64 bit wide data bus with an additional area penalty. The effectiveness of coding method has been tested using MATLAB. Transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA.

Keywords- *Inter-wire capacitance, substrate capacitance, low power switching.*

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I. INTRODUCTION

With technology enhancement in CMOS integrated circuit design power dissipation, cross-talk, size and delay has emerged as major issues to be considered. In any CMOS VLSI circuitry, the major sources of power dissipation [1][2] are identified as:

$$P_{diss} = P_{static} + P_{dynamic} + P_{leakage} + P_{shortckt} \quad (1)$$

The bus wires which are located close to each other, forms parallel plate capacitor known as inter-wire capacitance or coupling capacitance (C_c) which is more governing as compare to self or substrate capacitance (C_s) [2]. So in DSM technology more power is dissipated in the form of dynamic power for discharging and charging node capacitances [9]. This dynamic power is given by: [1]-[8]

$$P_{dynamic} = \alpha * V_{DD}^2 * f * C_L \quad \text{Watt} \quad (2)$$

Where:
α = Switching factor.
C_L = Load capacitance.
f = Frequency of operation.
V_{DD} =Supply voltage.

α is switching or transitioning factor. This switching factor depends on two types of transition as Self transition (α_s) and Coupling transition (α_c). Switching factor is given by:

$$\alpha = \alpha_s * C_S + \alpha_c * C_C \quad (3)$$

Here is the new expression for dynamic power dissipation in terms of Self and Coupling Transition-

$$P_{dyn} = [\alpha_s C_S + \alpha_c C_C] * V_{DD}^2 * f \quad \text{Watt} \quad (4)$$

C_s = Self or Substrate Capacitance
C_c = Coupling Capacitance or Inter-Wire Capacitance
f = Clock Frequency
V_{DD} = Supply Voltage
α_c = Coupling transition activity factor.
α_s = Self transition activity factor. [3][5][6]

Where,

$$P_{dyn} = \alpha_s C_s * V_{DD}^2 * f \quad \text{Watt} \quad (5)$$

is the dynamic power dissipation due to self-transition.

$$P_{dyn} = \alpha_c C_C * V_{DD}^2 * f \quad \text{Watt} \quad (6)$$

is the dynamic power dissipation due to coupling-transition and our aim is to reduce dynamic power dissipation due to coupling transition.

We know that the factors like V_{DD} and f are specific to a particular technology and cannot be altered for a particular purpose so therefore for reducing power dissipation, our main focus will be reducing the transition activity α as whenever a data bit is transmitted on a bus wire, the charging and discharging of this wire capacitance, self capacitance and coupling capacitance, results in power consumption.
Dual Coding Technique is introduced to reduce dynamic power dissipation by reducing Coupling Transition activity α_C. Techniques to reduce power dissipation were well explored in the literatures like [7] offers a TSC (Two Stage Coding) technique. Literature [8] introduced a technique in which data bus is first divided into two group as odd group and even group and then invert the data or send it as it is according to cases. Paper [9] developed a mathematical model for a memoryless encoding scheme and proposed a novel partitioning method for reducing the transition energy. Literature [10] explored a technique in which input data bits coded in four different ways such as Original Data, Invert Data, Ex-Oring with some code words and Ex-Oring with another code words and then send all the four results in comparator mode, which compares power dissipation value. The lowest of the four results decides the value of encoded

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data. Literature [11] proposed an octo coding technique to reduce the hamming distance, in which input data bits coded in eight different ways such as Invert, Swap, Invert even position, Invert odd position, Rotate left with invert, Rotate Right with invert, Circular Left Shift and Circular Right Shift based. Technique resulting in maximum reduction in power dissipation is selected. Technique introduced in paper [6] is Quadro Coding, in this method, the applied input data is coded in four different ways and the coding resulting in maximum reduction in transition activity is selected.

As in CMOS VLSI circuits, the dynamic power dissipation contributes a significant fraction in the overall power dissipation. In dynamic power dissipation it has been found that 75% of the power dissipation is due to the coupling capacitance whereas only 25% is due to self capacitance. The purpose of present paper is to propose a technique, Dual Technique, which attempts to reduce the number of effective coupling transitions (1 → 0 or 0 →1) between adjacent bus because in DSM technology the interconnect capacitance or coupling capacitance is more dominant than self one.

The rest of the paper is organized as follows: The bus model is explained in section II. The proposed model is well explored in section III. Methodology is explained in section IV. The results and discussions are provided in section V and conclusions are made in section VI.

II. BUS MODEL

A lucid bus line model [1][6] has been used to estimate dynamic power dissipation which in general consists of n number of parallel adjacent lines with a bus driver and number of repeaters as shown in figure 1.

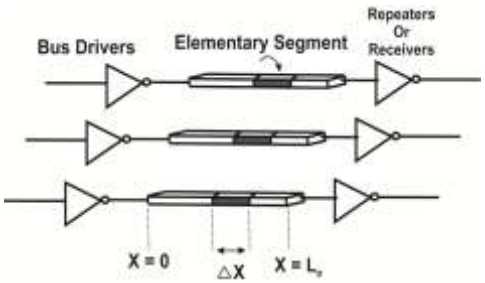

Fig.1. Bus Model

The distributed model of DSM bus line, in terms of RLC, is shown in fig.2. The bus lines can be assumed to be lossy, distributed, capacitively and inductively coupled which interact strongly with each other through parasitic capacitances and inductances. In the well-known model of DSM bus lines [12][13] the interconnect coupling capacitance C_C is strongly dependent on the inter–wire separation, whereas the lumped grounding capacitance C_S is a weak function of inter-wire separation.

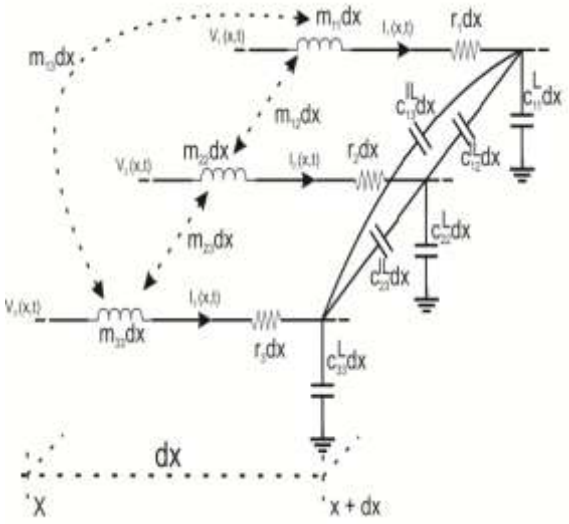

Fig.2. RLC Model for DSM Bus

The simple bus model including the effect of self-capacitance C_S from each bus line to ground and coupling capacitance C_C between two adjacent bus lines are shown in figure 3 [10][11][14]. Where V_1, V_2, V_3….V_n are the node voltages.

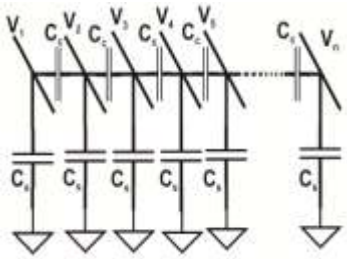

Fig.3. Self Capacitance and Coupling Capacitance in Bus Model

There are some limitations in previous method as no. of transitions was more so as dynamic power dissipation was very high.

III. PROPOSED MODEL

The main goal of the proposed scheme is to make data less correlated i.e. to make transitioning of data smoother. The proposed encoding scheme is as follows:

A. Encoder-

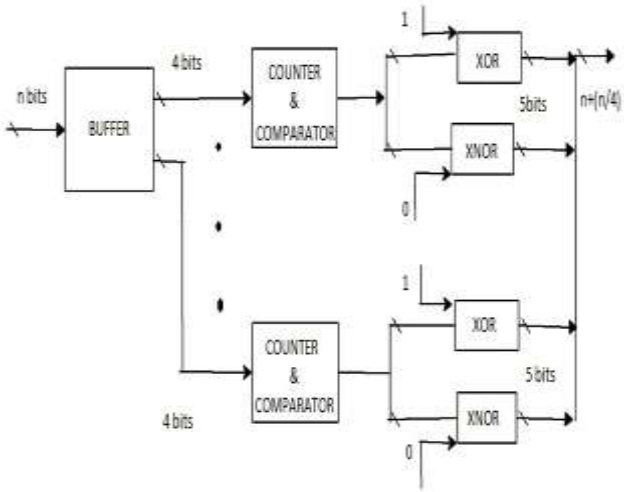

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Fig.4. Encoder for Dual Coding Technique

Let D be the n bit data on the bus to be transmitted at time t and X be the encoded data. The n bit data on the bus is divided into a subset of four bits from right to left and for each subset count the number of zeroes and ones. Now for encoding purpose nth (right most) bit is encoded as it is i.e. X(n)=D(n), and the following operations are performed to encode rest of data bits from right to left according to different conditions:

$$X(P) = D(P) \text{ XOR } X(P+1) \quad (7)$$

$$X(P) = D(P) \text{ XNOR } X(P+1) \quad (8)$$

Where P gives the position of the data bit varies from n-1 to 1. In the subset

- If number of 0's > number of 1's then operation (7) is applied in corresponding subset.
- If number of 0's < number of 1's then operation (8) is applied corresponding subset.
- If number of 0's = number of 1's then count the number of transition in subset and If
  - Number of transitions > 1 then operation (7) is applied in the corresponding subset.
  - Number of transitions =1 then operation (8) is applied in the corresponding subset.

Control bit 1 is associated with the subset if operation (7) is applied and 0 is associated if operation (8) is applied for decoding purpose. The control bit of each subset gives information about the operation performed on the corresponding subset. So due to control bit, length of encoded data X would be n+n/4.

B. Decoder-

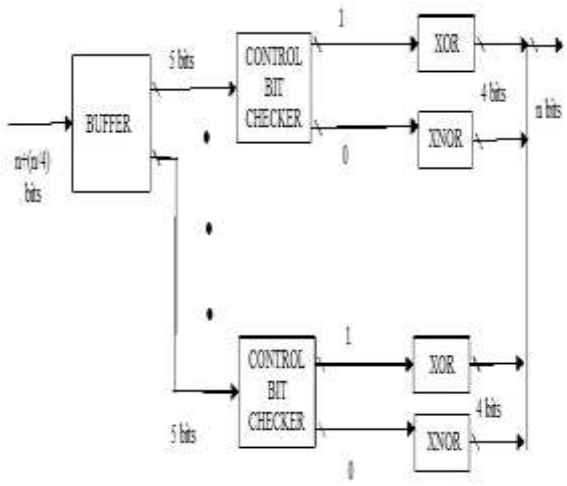

Fig.5. Decoder for Dual Coding Technique

For the decoding purpose encoded data is again divided into subsets from right to left. Then, nth bit is decoded as it is i.e. D (n) =X (n) and according to the control bit of each subset, original data is recovered by using anyone of the operation:

$$D(P) = X(P) \text{ XOR } X(P+1) \quad (9)$$

$$D(P) = X(P) \text{ XNOR } X(P+1) \quad (10)$$

Where P gives the position of data bit varies from n-1 to 1. If control bit of corresponding subset is 1 then operation (9) is applied and if it is 0 then operation (10) is applied.

IV. METHODOLOGY

In order to carry out the experiment and the target, following steps were involved.

1. Developed the MATLAB script for the encoder.
2. Developed the MATLAB script for the decoder.
3. Analysis of reduction in dynamic power dissipation using simulation tool MATLAB. For delay analysis, transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA.

V. SIMULATION RESULT AND DISCUSSION

A. Result Analysis for Dynamic Power Dissipation

The coding scheme is implemented and simulated using MATLAB tool. The simulation has been tested against approximately 10,000 different input vectors and it was observed reduction in coupling transition is guaranteed in most of the cases.

Table 1 shows the simulation results of 8 bits, 16 bits, 32 bits and 64 bits data and percentage reduction in dynamic power dissipation due to reduction in coupling transition:

TABLE I RESULTS OF DUAL CODING TECHNIQUE FOR DIFFERENT BUS WIDTH

Number of Bits in Data	Original Data	Number of Transitions in Original Data	Encoded Data	Number of Transitions in Encoded Data	% Reduction in Dynamic Power dissipation due to reduction in Coupling Transition
8	00001101	3	00000001	1	66.66
16	10110100 00101110	9	11000011 11100000	3	66.66
32	10111000 11010000 11111000 11110000	11	00111000 00011111 11111000 00000000	4	63.63
64	11110100 10010000 01000010 11110010 11101000 11110101 11110010 00011101	30	00000011 10001111 11000001 11111110 00001000 00000011 00000001 11110001	13	56.66

Using formula given in equation 6, we can calculate the dynamic power dissipation of NOC, due to coupling transition, designed on Xilinx with certain specifications:
Load Capacitance C_C = 1ηF,
Supply Voltage V_{DD} = 5 V,

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Operating frequency f = $193X10^6$ Hz.

For transitions i.e α_c, we have observed various conditions, number of transitions in original data and number of transitions in encoded data for different bus width. When we reduce the switching activity of NOC, using Dual Coding Technique, by that time we get reduction in dynamic power dissipation which can be calculated using formula given in equation 6. In this way we get the % reduction in dynamic power dissipation.

COMPARATIVE ANALYSIS

Following tables shows the comparison of proposed technique with different existing techniques for different bus width.

1. FOR 8 BITS →

Comparison Results for % Reduction in Power Using Memory less Interconnect Encoding Scheme, Novel Bus Coding for Nanometer Technology, Octo-Coding Method, Quadro Coding Technique and Proposed Dual Coding Technique.

TABLE II COMPARISON TABLE OF PROPOSED TECHNIQUE WITH DIFFERENT EXISTING TECHNIQUES FOR 8 BITS

Coding Techniques	% Reduction in Average Power	Proposed Technique	% Reduction in Average Power
Memory less Interconnect Encoding Scheme	22	Dual Coding Technique	66.66
Novel Bus Coding for Nanometer Technology	54	Dual Coding Technique	66.66
Octo-Coding Method	49	Dual Coding Technique	66.66
Quadro Coding Technique	36	Dual Coding Technique	66.66

We compare the results of proposed technique i.e. The Dual Coding Technique, with previous techniques for 8 bits bus width. Comparison graph is given below:

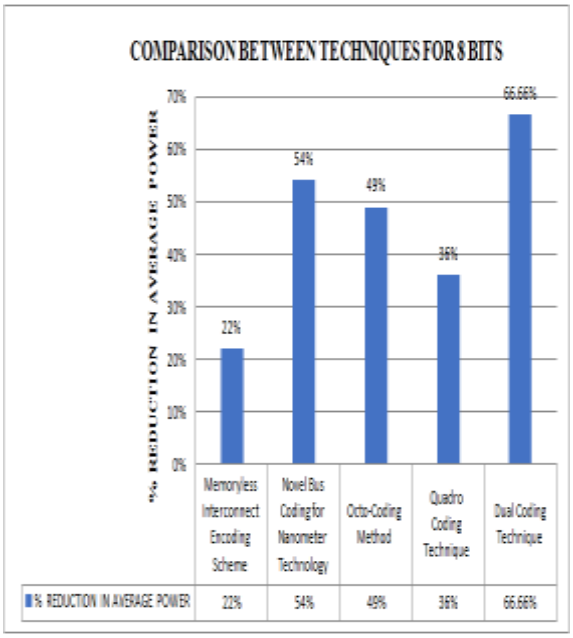

Fig.6. Comparison Between Proposed Technique and Different Previous Techniques for 8 Bits

From Fig. 6, we can easily conclude that we get maximum power reduction through this novel technique (Dual Coding Technique).

2. FOR 16 BITS →

Comparison Results for % Reduction in Power Using Novel Bus Coding for Data Transmission, Memory less Interconnect Encoding Scheme, Novel Bus Coding for Nanometer Technology, Octo-Coding Method, Quadro Coding Technique and Proposed Dual Coding Technique.

TABLE III COMPARISON TABLE OF PROPOSED TECHNIQUE WITH DIFFERENT EXISTING TECHNIQUES FOR 16 BITS

Coding Techniques	% Reduction in Average Power	Proposed Technique	% Reduction in Average Power
Novel Bus Coding for Data Transmission	24	Dual Coding Technique	66.66
Memory less Interconnect Encoding Scheme	20	Dual Coding Technique	66.66
Novel Bus Coding for Nanometer Technology	43	Dual Coding Technique	66.66
Octo-Coding Method	49	Dual Coding Technique	66.66
Quadro Coding Technique	23	Dual Coding Technique	66.66

We compare the results of proposed technique i.e. The Dual Coding Technique, with previous techniques for 16 bits bus width. Comparison graph is given below:

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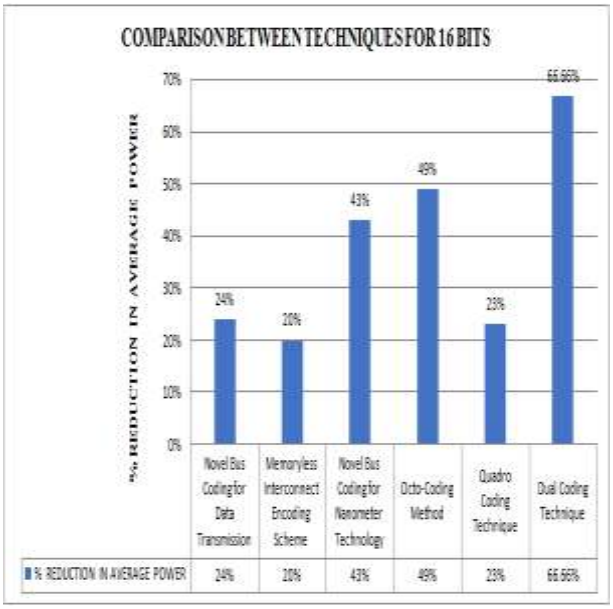

Fig.7. Comparison Between Proposed Technique and Different Previous Techniques for 16 Bit

From Fig. 7, we can easily conclude that we get maximum power reduction through this novel technique (Dual Coding Technique).

3. FOR 32 BITS →

Comparison Results for % Reduction in Power Using Novel Bus Coding for Data Transmission, Memory less Interconnect Encoding Scheme, Novel Bus Coding for Nanometer Technology, Octo-Coding Method, Quadro Coding Technique and Proposed Dual Coding Technique.

TABLE IV COMPARISON TABLE OF PROPOSED TECHNIQUE WITH DIFFERENT EXISTING TECHNIQUES FOR 32 BITS

Coding Techniques	% Reduction in Average Power	Proposed Technique	% Reduction in Average Power
Novel Bus Coding for Data Transmission	24	Dual Coding Technique	63.63
Memory less Interconnect Encoding Scheme	20	Dual Coding Technique	63.63
Novel Bus Coding for Nanometer Technology	32.10	Dual Coding Technique	63.63
Octo-Coding Method	49	Dual Coding Technique	63.63
Quadro Coding Technique	15	Dual Coding Technique	63.63

We compare the results of proposed technique i.e. The Dual Coding Technique, with previous techniques for 32 bits bus width. Comparison graph is given below:

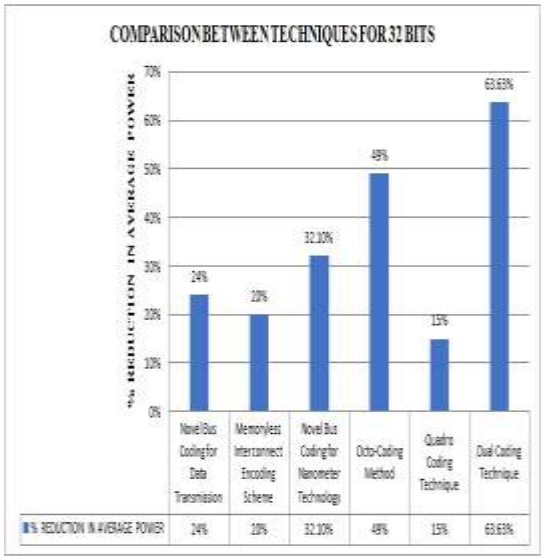

Fig.8. Comparison Between Proposed Technique and Different Previous Techniques for 32 Bits

From Fig. 8, we can easily conclude that we get maximum power reduction through this novel technique (Dual Coding Technique).

4. FOR 64 BITS →

Comparison Results for % Reduction in Power Using TSC Technique, Memory less Interconnect Encoding Scheme and Proposed Dual Coding Technique.

TABLE V COMPARISON TABLE OF PROPOSED TECHNIQUE WITH DIFFERENT EXISTING TECHNIQUES FOR 64 BITS.

Coding Techniques	% Reduction in Average Power	Proposed Technique	% Reduction in Average Power
TSC technique	17.34	Dual Coding Technique	56.66
Memory less Interconnect Encoding Scheme	21	Dual Coding Technique	56.66

We compare the results of proposed technique i.e. The Dual Coding Technique, with previous techniques for 64 bits bus width. Comparison graph is given below:

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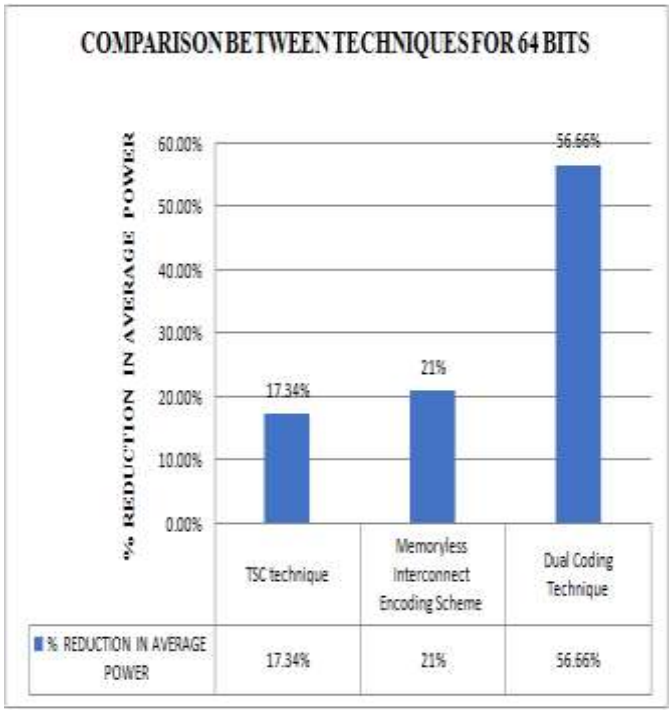

Fig.9. Comparison Between Proposed Technique and Different Previous Techniques for 64 Bits

From Fig. 9, we can easily conclude that we get maximum power reduction through this novel technique (Dual Coding Technique).

B. Result Analysis for Delay

For delay analysis, transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA. The simulation has been tested against approximately 10,000 different input vectors and it was observed delay reduction is guaranteed in all the cases. Table 6 shows the simulation results of 8 bits, 16 bits, 32 bits and 64 bits data and percentage reduction in delay:

TABLE VI RESULTS OF % REDUCTION IN DELAY FOR DIFFERENT BUS WIDTH USING DUAL CODING TECHNIQUE

Number of Bits in Data	Original Data	Delay (ns)	Encoded Data	Delay (ns)	% Reduction in Delay
8	00001101	2.853	00000001	2.464	13.63
16	10110100 00101110	4.968	11000011 11100000	4.322	13.00
32	10111000 11010000 11111000 11110000	6.247	00111000 00011111 11111000 00000000	5.396	13.62
64	11110100 10010000 01000010 11110010 11101000 11110101 11110010 00011101	9.758	00000011 10001111 11000001 11111110 00001000 00000011 00000001 11110001	8.435	13.55

VI. CONCLUSION

This paper presents a Dual Coding Technique which makes efforts to reduce dynamic power consumption due to coupling transitions in deep submicron (DSM) technology. The proposed technique simply uses XOR and XNOR operations according to conditions to achieve the objective. Results of Dual Coding Technique are very efficient and useful to reduce power dissipation up to 66.66% for 8-bit and 16 bit wide data bus, 63.63% for 32-bit wide data bus, 56.66% for 64-bit wide data bus and delay by 13% - 13.63% for 8 bit, 16 bit, 32 bit and 64 bit wide data bus with an additional area penalty.

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