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Comparison of Various Leakage Power Reduction Techniques for Full Adder Circuit

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Abstract: CMOS technology is the element in the development of VLSI systems because CMOS circuits consume very little power. Leakage power consumption in CMOS technology is a challenge in VLSI circuit designs. Leakage power dissipation is considered as total power consumption as technology feature sizes are reduced to nanometer in deep submicron technologies. This paper provides performances comparison analysis of single bit adder using transmission gate, CPL, sleep zigzag, zigzag keeper and sleepy keeper approach. To get low power during sleep or standby mode, the operating supply voltage can be disconnected to the rest of the circuit with an additional sleepy transistor. The objective of this paper is to present the review of various methods & techniques which are used for reducing the leakage power in VLSI circuits. All the proposed schematics are designed using TANNER EDA S-EDIT tool.

Keywords: - *CMOS, sub-threshold current, leakage power, sleep transistor, Low Power, Full Adder (FA).*

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1. INTRODUCTION

Today in VLSI technology leakage power dissipation plays an important role for low power VLSI designers. Today,The number of gates on a single chip are increased by which size of a device is reduced. The need for low power is not only because of the growing demands of mobile applications. But the area, power consumption have been a fundamental problem. To solve these problems, many researchers have been proposed so many techniques. Today the number of transistor on a particular area is still growing, which require cooling and packaging technologies. Which is very costly. In this condition reduction of the supply voltage is very effective to reduce the power consumption. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor. Sub-threshold operation of a transistor results into sub threshold leakage current, the main source power of leakage power. if the gate voltage of a transistor is lower than the threshold voltage (required voltage to turn ON the transistor), the transistor is not completely OFF and a small current still flows which is known as sub- threshold leakage current[1][13]

In VLSI design, the total power dissipation is divided in two parts (1) static power dissipation (2) dynamic power dissipation. Static power dissipation consists when there is no activity in a circuit or when circuit is in off mode but some power is dissipated that is called static power dissipation. Dynamic power dissipation consists either due to charging and discharging of load capacitance. [2][14]

In VLSI circuits there are several current components which are responsible for the leakage power dissipation. The Diagram of leakage current mechanism in a MOSFET is shown in below figure.

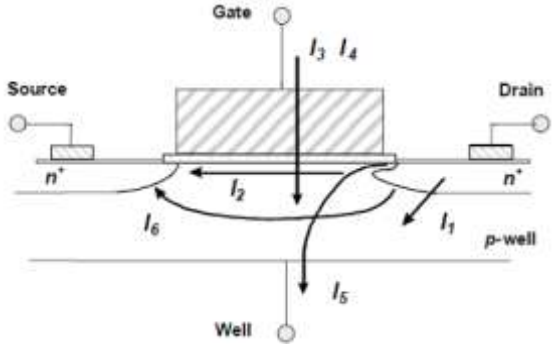

Fig.1. Leakage Current Mechanisms [21]

I1= Reverse-bias p-n junction diode leakage current
I2 = Sub-threshold leakage current
I3 = Gate Oxide tunneling current
I4 = Hot-carrier injection current
I5 = Gate induced drain-leakage current
I6 = Channel punch-through

The reverse bias p-n junction leakage (I1) is either due to minority carrier diffusion/drift near depletion region or due to electron-hole pair generation in depletion region. Sub-threshold leakage current (I2) is created when a gate voltage is not higher than the threshold voltage of the device, but due to short channel effect, there is some minor current in the device. Gate oxide leakage (I3) occurs due to the presence of high electric field across the oxide thickness which causes electrons to tunnel either from substrate to gate or gate to the substrate. Hot carrier injection (I4) results due to the lowering of the threshold voltage by electrons/holes. Gate-induced drain leakage (I5) current created due to the movement of minority carriers between channel and substrate regions. Punch through leakage (I6) is due to the current flowing between source and drain regions when channel disappears.[3]

To reduce leakage current, various leakage power reduction techniques have been proposed in this paper,

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which provides a new choice to the low leakage power VLSI designers. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique

2. LEAKAGE POWER REDUCTION TECHNIQUE

2.1 Transmission gate:

Fig.2. Schematic of Full Adder using Transmission gate

2.2 Complementary pass transistor (CPL):

In the above technology circuit complexity is increased so we used complementary pass transistor logic concept.. In this technology, we use only NMOS pass transistor. All inputs are applied in complementary form, every input signal and its inverse must be provided. The circuit also gives complementary output.[5][20]
The elimination of PMOS transistors in this reduces the parasitic capacitances associated with each node in the circuit. It provides high-speed, good driving capabilities. The advantage of this technology is that only one transistor (either NMOS or PMOS) is sufficient to perform the logic operation, which reduced the number of transistor and require low power consumption. But the disadvantages of this technology is that we can not get full swing at the output because NMOS transistor will be gone in cut off region when $Vg < V_t$.

2.3 Sleep approach:

One of the most commonly known approach for sub-threshold leakage power reduction is the sleep approach. In this technology, some additional transistors (sleep transistors) are inserted between the power supply and ground. The transistor which is placed between VDD and the pull-up network called "sleep" PMOS transistor and the transistor which is placed between pull-down network and the ground called "sleep" NMOS transistor.[6][16]

These sleep transistors turn off the circuit by cutting off the power rails. When the circuit is active, the sleep transistors are turned on so that it provides very low resistance in the conduction path and circuit's performance will not be affected due to these transistors. These transistors are turned off during the standby mode and provide large resistance in the conduction path so that leakage power is reduced in the circuit. This technique can reduce leakage power. This technique is also called gated- GND and gated-V_{DD} [7]

In below given figure a full adder is design by using sleep approach.

In transmission gate when a circuit is implemented by transmission gate, the main advantage of this technology is that we get a full swing at the out put. Because this technology contains NMOS as well as PMOS. Because PMOS will not go in cutoff region. It always goes either saturation or linear region.[19]
In this given below figure we implement full adder using transmission gate.[4][21]

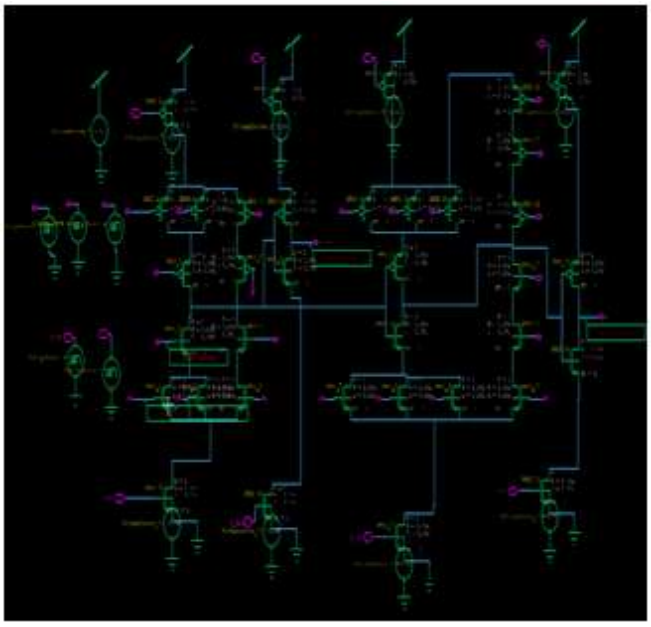

Fig.4. Schematic of Full Adder using sleep approach

2.4 Sleepy keeper Approach:

This approach uses leakage feedback technique. We know that PMOS transistors are not efficient at passing ground and NMOS transistors are not efficient at passing VDD. In this approach, a NMOS transistor is placed parallel to the sleep PMOS transistor and a PMOS transistor is placed in parallel to the sleep NMOS transistor[22].During sleep mode, sleep transistors will be turned off but the transistors that are in parallel to sleep transistor keep the contact with the appropriate power rail.[16][8]
In below-given figure a full adder is designed by using sleepy approach.

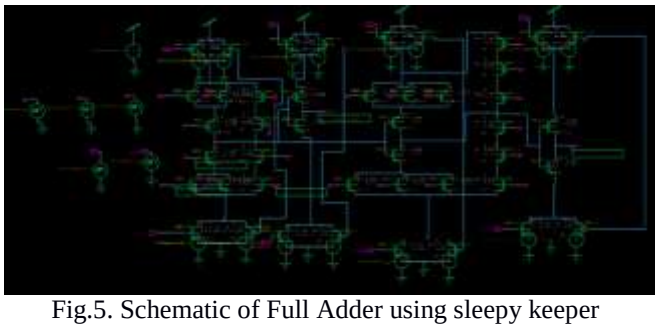

Fig.5. Schematic of Full Adder using sleepy keeper approach

2.5 Zigzag Approach:

This approach uses alternating sleep transistor in each logic stage either in the pull-up or pull-down network by which wake up delay can be reduced according to input vector. And it will help to achieve the lowest possible leakage

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power consumption.[9][10].This approach contains a less number of sleep transistor compare to sleep approach by which area is reduced. This approach has some limitation also that this technique requires some extra circuitry for generating a specific input pattern.

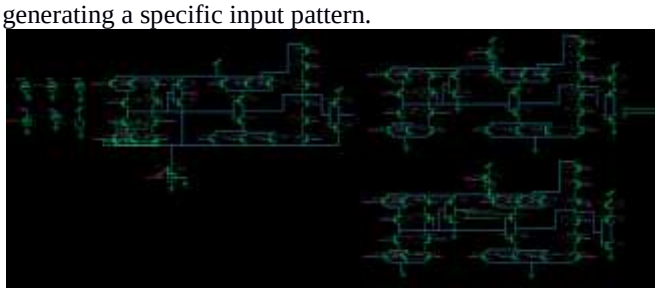

Fig.6. Schematic of Full Adder using Zigzag approach

2.6 Zigzag keeper Approach:

Another important technique is "zigzag with keeper". This technique contains the sleep transistor with two additional transistors driven by already calculated output which retains the state of the circuit during the sleep mode. **[11][12]**

In below-given figure a full adder is designed by using Zigzag keeper approach.

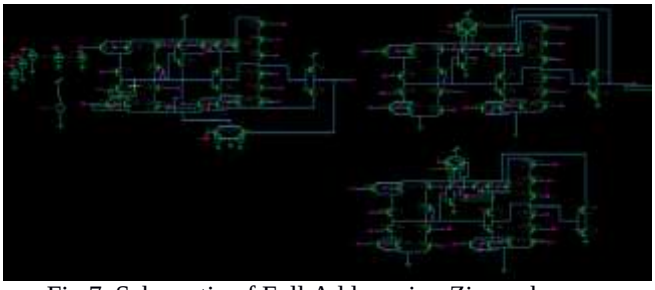

Fig.7. Schematic of Full Adder using Zigzag keeper approach

3. RESULTS:

This section contains the result of a full adder for the different parameter like power consumption, delay, power product delay by using different leakage reduction technology. This is shown in below -given table.

Table 3.1 comparison chart of all parameter

S. No.	Techniques	Power consumed	Delay		Power delay product	
		(µW)	Sum (ns)	Carry (ns)	Sum (10^{-15})	Carry (10^{-15})
1.	Transmission gate	47.6	0.02	0.12	0.95	5.71
2.	CPL	52.4	0.18	0.21	9.43	11.01
3.	Sleep Transistor	44.2	0.35	0.27	15.47	11.93
4.	Sleepy keeper	16.0	0.26	0.41	4.16	6.56
5.	Zigzag	99.7	0.44	0.38	43.86	37.88
6.	Zigzag keeper	45.1	0.26	0.37	11.72	16.68

4. CONCLUSION

From the above- given table, it shows that zig -zag technique has very large power consumption, and transmission gate technique has a very low delay but if we consider all parameter sleepy keeper approach has a very effective and it has a very low power consumption as well as delay also. The result is simulated with TANNER software.

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