Survey on Linear Phase Reconfigurable Filters for Software defined Radio

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Abstract— Since there are different telecommunication standards, communication engineers main focus turns to design flexible radio system to handle different service. As the ways and means by which people need to communicate data, voice, video communication, broadband messaging, command and control communication, and emergency response communication are increases exponentially. Software defined radio (SDR) is a technology that brings flexibility in communication to support multiple channels of different communication standard. Reconfigurable type techniques are used in SDR like designs. SDR receivers use reconfigurable digital filters (RDFs) to perform multi standard channelization, i.e., extraction of desired radio channels (frequency bands) from a wideband input signal. The most important unit in transceiver is digital front end (DFE).DFE Perform operation like channelization, sample rate conversion, digital down conversion .Digital filter bank is used to extract multiple radio channels from wide band input in channelizer. Ideally the reconfigurabilty of the filter accomplished by reconfiguring the same prototype filter in the filter bank instead of employing separate filter banks for each standard. The realization of dynamically reconfigurable linear phase filter with sharp transition width and low complexity is really a challenging task. There are different types of RDFs ,The study gives a brief description of different types of RDFs and how the reconfigurabilty is achieved in the design.

Keywords— *RDF,linear phase, Software Defined Radio(SDR), Frequency response masking(fFRM).*

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I. INTRODUCTION

Current focus among communication engineers is to design flexible radio systems to handle services among different telecommunication standards. Such communication system use different bandwidths, from different telecommunication standards. The formatter will need to create these components, incorporating the applicable criteria that follow. The advancements in mobile communications have also made

prominent impact on improving education, health, public Safety disaster management, banking services etc [1]. The radio transceivers that support multiple communication standards have distinct architectures for distinct standards. This causes high resource utilization and thus high power consumption. Software Defined Radio has been proposed as a solution for this problem. Software Defined Radio (SDR) is emerging as a promising technology to use a general purpose hardware which can support the various existing and future communication standards. The transceivers in SDR can be reconfigured to support multiple communication standards through software reconfiguration. The block diagram of an SDR receiver is shown in figure 1.

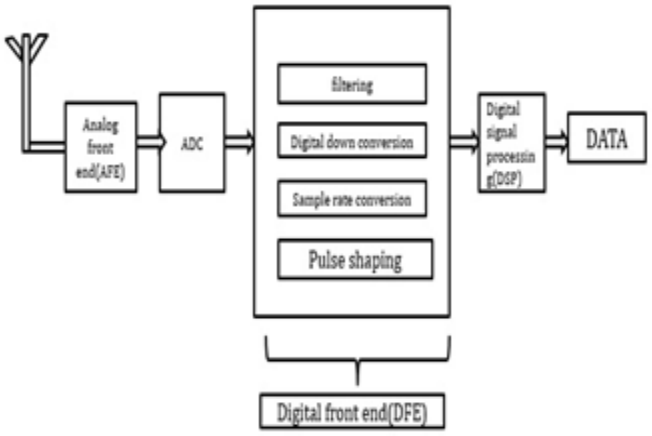

Figure1. SDR receiver

The DFE is one of the most computationally intensive blocks of the MWCR. In Emerging SDRs and CRs, the DFE along with the DSP algorithms are required to perform two main tasks: Channelization(Extraction of individual channel(s) of distinct bandwidth and locations from the wideband input signal)and Spectrum sensing(Detecting the presence and absence of channel vacant frequency band(s)) in the wideband input signal [2]).

The MWCR architecture consists of four serial blocks which are: Analog front end (AFE), Analog-to-digital Convertor (ADC), Digital front end (DFE) and Digital signal processing (DSP) algorithms as shown in Figure.DFE is responsible for extracting the desired channel(s) of interest from the wideband

digitized intermediate frequency signal. To accomplish this, the DFE needs to perform various tasks such as channel filtering, digital down conversion to bring the channel(s) to DC, sample rate conversion to decimate the signal to the standard specific symbol rate, pulse shaping etc. Out of these, digital filtering is a key task of the DFE since it is the first task in the MWCR which takes into account the type of communication standard and involves a large number of computationally expensive arithmetic operation multiplication and addition operations.

II. LINEAR PHASE FILTER

The procedure of changing associate degree analog signal into digital signal is performed victimization sampling with a finite frequency fs. Linear phase filters are mainly used in communication oriented applications. A linear phase filter will preserve the wave shape of the signal or component of the input signal (to the extent that's possible, given that some frequencies will be changed in amplitude by the action of the filter). This could be important in several domains like coherent signal processing and demodulation, audio processing etc.

A. Types of filter

Filters are often classified into completely different teams supported the necessity. In the main finite impulse response (FIR) and infinite impulse response (IIR)[3] filters are used. Each kinds of filters have their own benefits and drawbacks that play a significant role whereas planning filter. Fir filters offer linear phase characteristics, forever stable but its disadvantage is it have higher complexity. On the opposite hand, the IIR filter provides nonlinear section characteristics, unstable and that they square measure used for fewer complexness. But fir filter realized using transposed direct form will reduce implementation complexity and produce high throughput without adding extra pipeline registers. So for linear phase and for reduce complexity transposed form of FIR filter is used.

III. DESIGN METHOD RECONFIGURABLE DIGITAL FILTERS

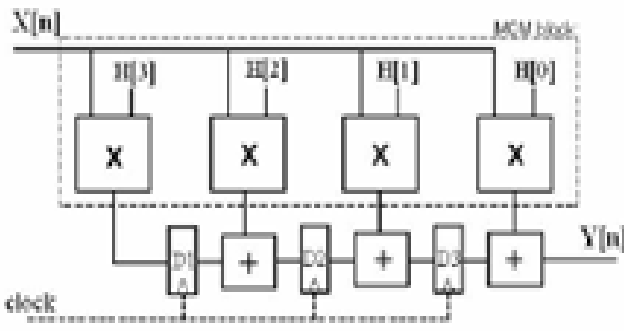

Figure 2: transposed 4 tap fir filter

A. Programmable filters(CSM& PSM method)

A CSM (constant shift method) and PSM (programmable shift method) based FIR filter architectures were proposed in [4].Thismethod was proposed as a low complexity reconfigurable filter structure which can be used for channelization in SDR. In this method the filter coefficients were considered as constants (as they are stored in LUT) and the input signal as variable. In CSM the FIR filter is implemented by partitioning the filter coefficients into fixed groups. In PSM the filter coefficients are coded in specific format in order to reduce the complexity by using BCSE algorithm. In this method reconfigurabilty is achieved by changing the LUT contents according to the communication standards involved which incurs high memory requirement and reconfiguration time. This makes it unsuitable for multi standard operation.

B. per-channel based approach

The term of the PC approach[5] is shown in figure 3. In figure 3 the order of channelization is filtering (H0(z) to Hn(z), digital down conversion (DDC), sample rate conversion (SRC) and finally baseband processing (BBP).The filter, H0(z), is a low pass filter and all other filters, H1(z) to Hn(z)), are band pass filters. It is possible to do digital down conversion followed by filtering and consequently, all the filters will be low pass filters (all filters are H0(z)). It is also possible to further reduce the complexity of the PC approach by employing polyphase decomposition of each of the filters and then moving the SRC to the left of filtering operation (i.e., performing SRC before filtering).By employing polyphase decomposition, the speed of filtering operation can be relaxed.

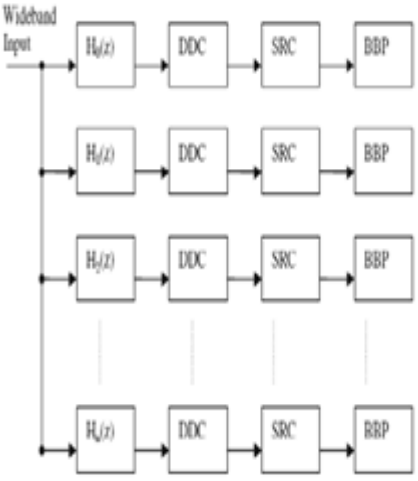

Figure 3: PC based filter diagram

The PC approach is a straightforward approach and hence relatively simple. But the main drawback is that, the number

of branches of filtering-DDC-SRC is directly proportional to the number of received channels i.e. the complexity of the PC approach is directly proportional to the number of channels. Hence the PC approach is not efficient when the number of received channels is large. The filters used in the PC approach are of a very high order and this results in high area complexity and thus increased static power[5].

C. Discrete Fourier transform filter bank (DFTFB)

Discrete Fourier transform filter bank (DFTFB) is widelyemployed. DFTFB is a modulated filter bank which consists of a single low pass filter followed by DFT operation [6]. The drawback of DFTFBs is that it cannot extract channels with different bandwidths simultaneously. Therefore, for multi-standard receivers, distinct DFTFBs are required to adapt to each communication standard. Hence, the complexity of the channelizer increases linearly with the number of standards.

M	N	N_{MA}	N_{MC}	$N+ N_{MA+} N_{MC}$	Effective length
2	200	1	26	227	424
3	134	5	33	172	432
4	100	13	19	132	415
11	37	64	33	135	660
12	36	93	34	160	689
13	31	30	33	254	583

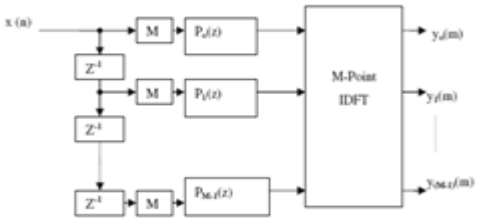

Figure 4: DFTB based filter architecture

D. Constant Multiplier Architecture Based on VHBCSE

An efficient constant multiplier architecture based on vertical-horizontal binary common sub-expression elimination (VHBCSE) algorithm for designing a reconfigurable finite impulse response (FIR) filter whose coefficients can dynamically change in real time. To design an efficient reconfigurable FIR filter, according to the proposed VHBCSE algorithm, 2-bit binary common sub-expression elimination (BCSE) algorithm has been applied vertically across adjacent coefficients on the 2-D space of the coefficient matrix initially, followed by applying variable-bit BCSE algorithm horizontally within each coefficient. This technique is capable of reducing the average probability of use or the switching activity of the multiplier block adders[7].In FIR filter, the multiplication operation is performed between one particular variable (the input) and many constants (the coefficients) and known as the multiple constant multiplication (MCM).

E. Frequency response masking method

The increase in complexity due to the use of variable coefficients can be reduced if the prototype filter coefficients are kept fixed and variable frequency responses are obtained by performing suitable mathematical operations on them using a small set of variable parameters. [8]. The block diagram of FRM RDF is shown in figure 5. It consists of a low pass prototype filter Ha(z) having an odd filter order N. The complementary filter of the prototype filter can be obtained by subtracting the output of Ha(z) from a suitably delayed version of the input. It can be represented as

$$H_c(z) = z^{-[(N-1)/2]} - H_a(z) \quad \text{.....(1)}$$

The prototype filter and the complementary filter are interpolated by a factor I to get the corresponding multi-band responses Ha(zm) and Hc(zm) respectively. From these interpolated frequency responses, the unwanted sub bands are masked by cascading suitable low order frequency response masking filters Hma(z) and Hmc(z) as shown in Figure 3. This operation gives the technique its name FRM. The output of the RDF shown in Figure is represented as

$$Y(z) = \{H_a(z^m).\ H_{ma}(z) + [z^{-I[(N-1)/2]} - H_a(z)]\ H_{mc}(z)\}\ X(z) \quad \text{.(2)}$$

Different types of multi-band frequency responses are generated using different values of the interpolation factor I and appropriate masking filters are used to extract the desired sub bands

TABLE 1: comparison of different values of M

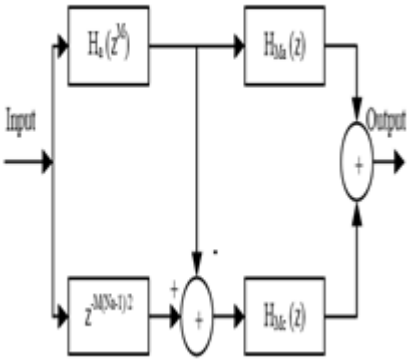

Figure 5: FRM architecture

By appropriate selection of the frequency response specifications (pass band and stop band edge frequencies) of the prototype filter and the masking filters, a frequency response with a sharp transition-band width can be obtained. It is known that the Complement of a zero-phase filter can be derived by subtracting the zero-phase filter In question from the unit impulse. This can be extended to causal odd-length FIR Filters by subtracting the causal filter in question from a delayed impulse equal to the Delay of the causal filter. The complementary filter has pass bands where the model filter has stop bands, And vice versa. Figure 6shows the two complementary un sampled filters together, and also

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shows that they sum to one.The frequency response is as shown in figure 7. The FRM technique provides variable low pass, high pass, band pass and band stop frequency responses using the same set of prototype filter coefficients. Thus, the implementation complexity of thFRM technique is low compared to the programmable filter implementationtechnique.

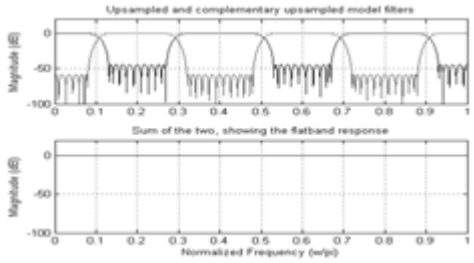

Fig ure6: FRM Complementary model filters and their

DESIGN MATRIX	ORDER	PC Approach[5]	DFTFB [6]	**FRM BASED FILTER[8]**
Area(mm) [13]	137	50.738	23.20	**7.579**
Delay(ns)[13]	137	43	32.4	**18.65**
Power(mW)[13]	137	106.5	78.3	**58.36**
Multiplication complexity rate[13]		Proportional to NI	Proportional to NI	**Less**
Gate count		569645	---	**380992**
Data arrival time(ns)		77		**38.6752**
Sampling frequency	137	12		**24**
Power dissipation[13]	137	2235		**558.77**
Silicon cost		poor	Very high	**Low**
Initial flexibility		yes	no	**Yes**

Sum

TABLE 1: comparison of different values of M

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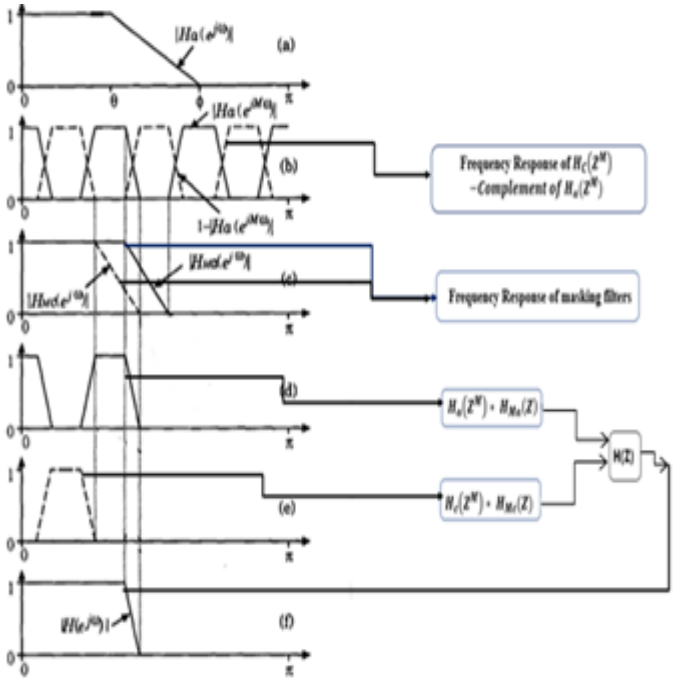

Figure 7: Frequency responses of FRM sub filters

While we choosing integer M certain factors should be considered. The algorithm used to calculate the M vector is not optimal. Because the values of M are restricted to integer values, the optimization problem is interesting and difficult. The right integer optimization technique may find a more optimal solution for the selection of the M vector[9]. Table 1 The interpolation factor 4 makes the implementation of the filter having less order that implies less number of adders and multipliers so complexity of design get reduced and hardware overhead will also reduce.

III.COMPARIOSN OF DIFFERENT TYPE FILTER

TABLE 2:comparison of different design methods

From the table 2 we can analyses that frequency response masking is the best method to implement low complexity reconfigurable filter. the delay, area, power of FRM based approach is less compared to PC approach and DFTB approach.But there is some problem in FRM technique, Complexity of interpolation structure is high and Increase hardware overhead when large number of channels is realized. so try to reduce the hardware overhead in FRM

technique.

IV.CONCLUSION

The benefit of FRM FIR filters is that the number of arithmetic operations required can be substantially smaller, because of the zero-valued impulse response values of the periodic model filter This technique produces filters with very sparse coefficients and so the resulting filter has very low arithmetic complexity. Low complexity increase the speed of filtering operation. In FRM compose the overall sharp transition-band filter using several wide transition-band sub filters. So the resultant filter will offer guaranteed stability and signal is free of phase distortion. Computational complexity of the whole system is same for the entire range of operating bandwidth.

REFERENCES

[1] Mitola J., "Software radio architecture: a mathematical perspective," IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 514-538, Apr. 1999

[2] Qing Z., Sadler B. M. (May 2007)" A survey of dynamic spectrum access", IEEE Signal Processing MagazineVol.24, Issue 3, pp.79-89.

[3] Daitx, Fábio Fabian, et al. "VHDL generation of optimized FIR filters." Signals, Circuits and Systems, 2008. SCS 2008. 2nd International Conference on. IEEE, 2008.

[4] R. Mahesh and A. P. Vinod, ―New reconfigurable architectures for implementing filters with low complexity,‖ IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 29, no. 2, pp. 275–288, Feb. 2010.

[5] R. Mahesh and A. P. Vinod, "A new common subexpression elimination algorithm for realizing low complexity higher order digital filters," IEEE Trans. Computer-Aided Design Integr, Circuits Syst., vol. 27, no. 2, pp. 217–229, Feb. 2008.

[6] Abu-Al-Saud, Wajih A., and Gordon L. Stuber. "Efficient wideband channelizer for software radio systems using modulated PR filterbanks." IEEE transactions on signal processing 52.10 (2004): 2807-2820.

[7] Hatai, Indranil, IndrajitChakrabarti, and Swapna Banerjee. "An efficient constant multiplier architecture based on vertical-horizontal binary common sub-expression elimination algorithm for reconfigurable FIR filter synthesis." IEEE Transactions on Circuits and Systems I: Regular Papers 62.4 (2015): 1071-1080.

[8] Mahesh, R., and A. Prasad Vinod. "Reconfigurable frequency response masking filters for software radio channelization." IEEE Transactions on Circuits and Systems II: Express Briefs 55.3 (2008): 274-278.

[9] Lim, Yong. "Frequency-response masking approach for the synthesis of sharp linear phase digital filters." IEEE transactions on circuits and systems 33.4 (1986): 357-364.