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A Leakage Compensation Design for SRAM

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Abstract—SRAM has an important role in many products,eg the cache of CPU. To extend the operation time and reduce power dissipation, Static Random-Access Memory (SRAM) is usually fabricated using advanced processes. Therefore, to reduce the leakage and increase the operation speed, a leakage current compensation circuit is designed for nanoscale SRAMs. The compensation design is composed of a leakage current sensor,which generates a warning signal if the leakage is over a predefined threshold, and a compensation circuit following the sensor, which will be activated to speed up the read operation. The simulation software Cadence is used to assist the design of the leakage compensation circuit.

Key Terms—*Compensation circuit,disturbfree, leakage sensor, single-ended Static Random- Access Memory cell, SRAM*

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I. INTRODUCTION

SRAM has an important role in many products, e.g., the cache of CPU. To extend the operation time and reduce power dissipation, Static Random-Access Memory (SRAM) is usually fabricated using advanced processes. However, as the technology is evolving towards the nanometer scale, the leakage becomes a threat.Scaling the supply voltage decreases the power consumption , but increases the delay of the circuit.Therefore the threshold voltage is reduced to reduce the circuit delay. The operation frequency and the power consumption of SRAMs will be deteriorated, because the leakage current increases exponentially with the drop of threshold voltage (Vth) and gate oxides.The drain-to-source current is composed by drift current and diffusion current. The drift current is the dominant mechanism in strong inversion regime, when the gate-to-source voltage exceeds the Vth. In weak inversion, the minority carrier concentration is almost zero, and the channel has no horizontal electric field, but a small longitudinal electric field appears due the drain-to-source voltage. In this situation, the carriers move by diffusion between the source and the drain of MOS transistor. Therefore, the subthreshold current is dominated by diusion current and it depends expo-nentially on both gate-tosource and threshold voltage. Although the high Vth CMOS has been deemed as a solution to the mentioned issues, it will slow down the operation speed of SRAMs.Therefore,to reduce the leakage and increase the operation speed a new compensation design is proposed. The proposed circuit iscomposed of a leakage current sensor and a compensation circuit. A leakage current sensor is utilized to sense the voltage drop caused by the leakage current. A compensation circuit will speed up the read operation of SRAM if the leakage is detected and confirmed.

II. BACKGROUND

A. 5T SRAM

In a normal 6T cell both storage nodes are accessed through NMOS pass-transistors. This is necessary for the writing of the cell since none of the internal cell nodes can be pulled up from a stored ’0’ by a high on the bitline.If this was not the case an accidental write could occur when reading a stored ’0’.How- ever, if the bitlines are not precharged to Vccthis is no longer true. With an intermediate precharge voltage, Vpc, the cell could be constructed so that a high on the bitline would write a ’1’ into the cell, but a precharged bitline with a lower voltage would not. Also a low on the bitline could write a ’0’ into the cell, whereas the intermediate precharge volt- age would not, thus giving the cell a precharge voltage window where correct operation is assured. This would eliminate the need for two NMOS transistors, since the cell now can be written both high and low from one side. In turn, that would also result in one less bitline. From a high density point of view this is very attractive as shown in fig 1

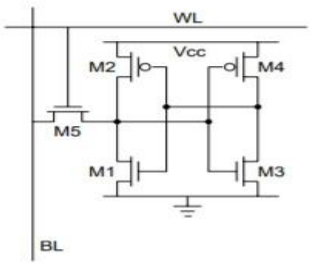

Figure1.5T SRAM

B. 6T SRAM

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A low power SRAM cell may be designed by using crosscoupled CMOS inverters. The most important advantage of this circuit topology is that the static power dissipation is very small;essentially,it is limited by small leakage current. Other advantages of this design are high noise immunity due to larger noise margins,and the ability to operate at lower power supply voltage.The major disadvantage of this topology is larger cell size. The circuit structure of the fullCMOS static RAM cell is shown in figure2.

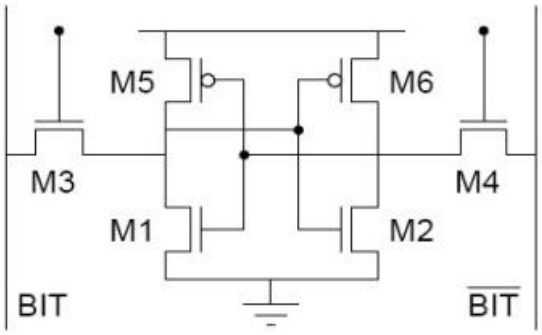

Figure2. 6T SRAM

C. *8T SRAM*

The fundamental stability problem in 6T cells is that in the read condition, a pass-gate pulls the ” storage node up to a nonzero value.Adding two FETs to a 6T cell provides a read mechanism that does not disturb the internal nodes of the cell,thereby eliminating the worst-case stability condition. This requires separate read and write word lines and can accommodate dual-port operation with separate read and write bit lines.

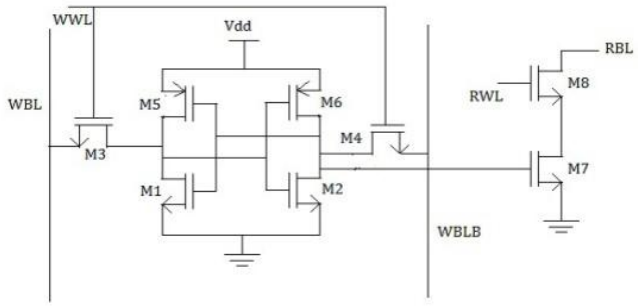

Figure3. 8T SRAM

D. *9T SRAM*

A 9T bit cell with enhanced write ability is achieved by inserting a pass transistor into the cross-coupled inverter pair is shown in fig 2.9. To allow the bit-interleaving array

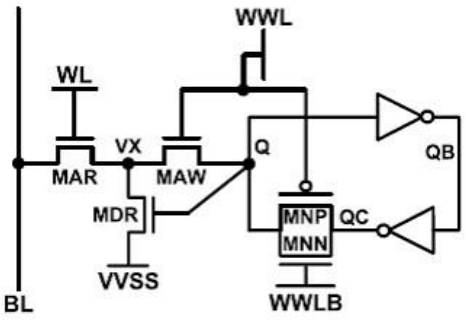

Figure4. 9T SRAM

scheme for 9T bit cells, two additional write wordlines (WWL/WWLb) are used. It adapts multiple threshold CMOS technique, including high Vt and regular Vt devices to deliver the benefits of saving leakage and increasing write margin (WM)/hold SNM (HSNM), respectively. Three n-type transistors, i.e., MAR, MAW, and MDR, construct the access buffer. Their device length increases to 100 nm, utilizing reverse short-channel effect for better aspect ratio and less threshold voltage variation caused by random dopant fluctuation.

III. DESIGN

The compensation design is composed of the leakage current sensor and compensation circuit.To reduce the leakage and increase the operation speed a new compensation circuit designed. The circuit is composed of a leakage current sensor and a compensation circuit. A leakage current sensor is utilized to sense the voltage drop caused by the leakage current. A compensation circuit will speed up the read operation of SRAM if the leakage is detected and confirmed..

A. Leakage Current Sensor

A leakage current sensor consists of an SRAM cell model and a comparator as shown in fig 5 . Since a large leakage will result in low operating frequency, high power consumption, and even status in the SRAM cell, an SRAM cell model is used as a leakage monitor generating a voltage proportional to the leakage current, vleakage, for comparator. If vleak- age is higher than vref, comparator will notify a warning signal to activate the following compensation circuit.We couple the node Q of 32 SRAM cells together and turn OFF all transistors to serve as the SRAM cell model.

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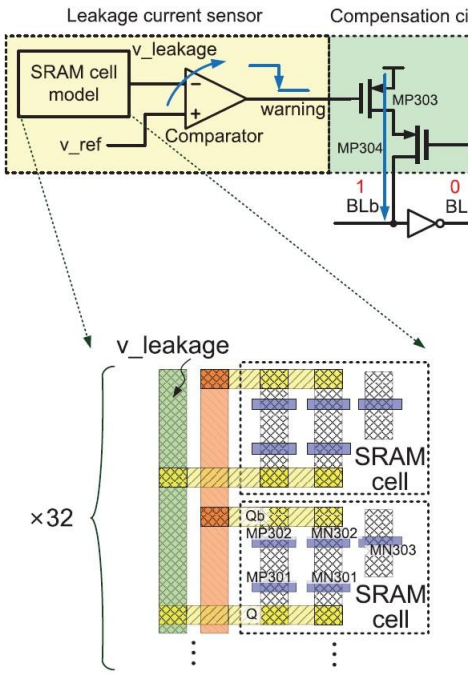

Figure 5.Compensation Circuit

B. *Comparator*

Fig.6 shows the schematic of comparator, which is basically a differential comparator to compare vleakage with a predefined reference voltage, vref. Notably, vref plays a critical role in the design..

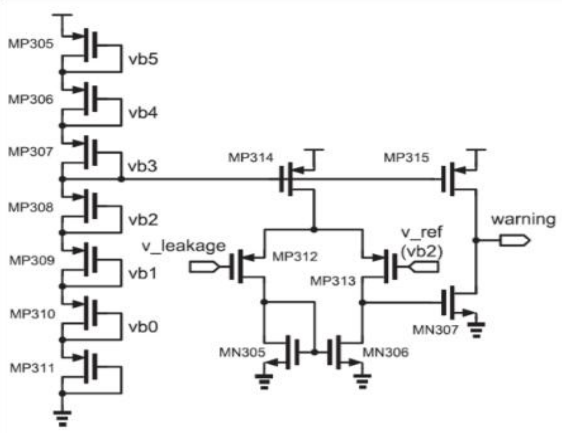

Figure6. Comparator

However, during the read 0 operation BLb will be pulled up due to few leakage owing from BLb to nodes Q and Qb. It may interfere the stored bit in the unaccessed SRAM cells if the time of the read 0 operation is too long. This syndrome becomes very serious when the entire circuit is operated at fast pMOS corner, since the leakage current of the pMOS is higher than that of nMOS.Once the output voltage of the SRAM cell model is higher than the voltage Compensa- tion circuit must be activated. Then, vb2, about 350 mV, in the MOS string of comparator in Fig. 6 is selected and coupled to vref. Notably, vleakage also depends on the SRAM cell size, which means we can appropriately select vref to be one of the six biases, vb0-vb5, according to the size of the SRAM cell model.

C. *Read Delay Compensation*

Referring to Fig.5 again, the details of the leakage compensation are as follows. 1) Step 1: vleakage rises to indicate that the SRAM cell model is suered from leakage currents. 2) Step 2: Once if vleakage is higher than vref, comparator pulls low the warning signal. 3) Step 3: As soon as the warning drops, MP303 in compensation circuit is turned ON to pullup BLb such that BL drops fast. In other words, a positive feedback is used to speed up the read access. The leakage will slow down the entire read access, especially in the scenario of state 0 is to be read. Therefore, a compensation circuit consisting of two pMOS keepers, MP303 and MP304, speeds up the read operation such that the inverter and the following logic circuits can quickly pass the triode region to reduce power dissipation. Notably, since the BLb will be predischarged at the beginning of each read operation, this compensate operation only operates, while data bit 0 is accessed. When reading data bit 1, it stays the same. Besides, the charging speed of the proposed compensation circuit is determined by the size of MP303 and MP304.

IV. DISCUSSION & RESULTS

The configurations of different SRAM's are implemented in cadence virtuoso tool .The wave- forms obtained after simulation during read operation is analysed and the delay is calculated.Compensation design with leakage current sensor and compensation circuit is shown in fig 5.7.As the leakage

Table I Read delay measurement results

Configurations	Delay without Compensation Circuit(ns)	Delay with Compensation Circuit(ns)
5T SRAM	62.5	59.4
6T SRAM	72.82	70.1
8T SRAM	77.72	75.6
9T SRAM	98.85	96.31

(470mv) is greater than reference voltage (350mv) the input at the in- verting terminal is greater than non invertimonal which produces an output of low voltage at the comparator which in turn ,turns ON the PMOS in the compensation circuit which pulls up the BLbar voltage which is connected

to an inverter which produces the complimentary output which is the BL.

Using compensation circuit the waveform of BLbar and

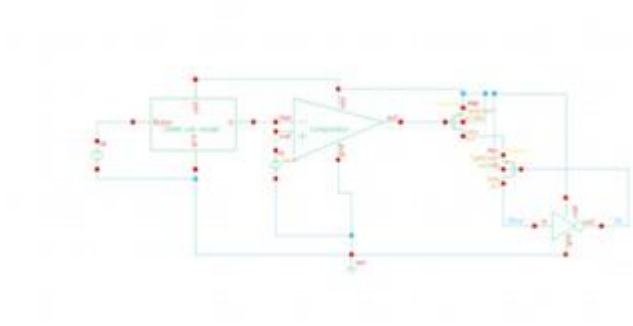

Figure 7. Compensation Circuit

BL are obtained as shown in fig .The inverted waveform is produced.By ,measuring the delay of the waveform the value obtained is 59.4ns.When compared to previous value there is a reduction in the delay by a value of 3.1 ns.

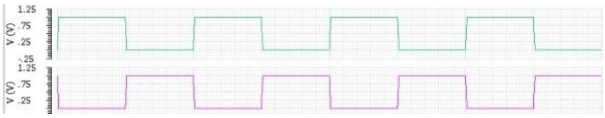

Figure8. Compensation Circuit

Table I provides the comparison of delay of various configurations when the compensation circuit is introduced.From the analysis we can see that the delay has decreased from the previous without compensation circuit.

V. CONCLUSIONS

The compensation design is composed of a leakage current sensor and a compensation circuit. The leakage current sensor can sense the voltage drop caused by the leakage current. As soon as a warning signal issued by the leakage current sensor is over a predefined threshold, the compensation circuit speeds up the read operation. By the measurement results given 1.2 system voltage it can be concluded that the read delay of various configurations has been reduced by the introduction of the leakage compensation design.

VI. APPENDIX

Cadence is an Electronic Design Automation (EDA) environment that allows integrating in a single framework different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment.

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