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Sub threshold 8T SRAM Cell with Dynamic Feedback

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Abstract— The Embedded memory,which is considered as an inevitable part of microprocessor controlled devices represents a large portion of the system-on-chip(SoC).These portable systems need ultra low power consuming circuits to utilize battery for a much longer duration.An 8-transistor(8T) static random access memory cell with improved data stability in subthreshold operation is implemented in Cadence virtuoso 45 nm Technology.The single-ended design is used to reduce the differential switching power during read and write operation.The power consumed during switching of data on single bit line is lesser than that on differential bit line pair.The single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultra low power supply.A comparative study between four SRAM cell structures such as conventional 6T SRAM,Read decoupled 8T SRAM,conventional 9T SRAM and Single Ended Dynamic Feedback Control SRAM in terms of SNM and power consumption for a VDD of 2V and 300mv in both 45nm and 90 nm is carried out.The SEDFC 8T possesses a high SNM with a reduced power consumption in subthreshold regime when compared with the other three SRAM cell structures.

Index Terms— *Subthreshold regime,Static Noise Mar- gin,Power consumption,Embedded memory,Cadence Virtuoso*

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I. INTRODUCTION

Random-access memory is a form of computer data stor- age that stores data and machine code currently being used. A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In contrast, with other direct-access data storage media such as hard disks, CD-RWs, DVD-RWs and the older magnetic tapes and drum memory, the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.RAM contains multiplexing and demultiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be ”8-bit” or ”16-bit”, etc. devices.[2] In today’s technology, random-access memory takes the form of integrated circuits. RAM is normally associated with volatile types of memory (such as DRAM modules), where stored information is lost if power is removed, although non-volatile RAM has also been developed[4]-[6], Other types of non-volatile memories exist that allow random access for read operations, but either do not allow write operations or have other kinds of limitations on them.

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The two widely used forms of modern RAM are static RAM (SRAM) and dynamic RAM (DRAM). In SRAM, a bit of data is stored using the state of a six transistor memory cell. This form of RAM is more expensive to produce, but is generally faster and requires less dynamic power than DRAM. In modern computers, SRAM is often used as cache memory for the CPU. DRAM stores a bit of data using a transistor and capacitor pair, which together comprise a DRAM cell. The capacitor holds a high or low charge (1 or 0, respectively), and the transistor acts as a switch that lets the control circuitry on the chip read the capacitor’s state of charge or change it. As this form of memory is less expensive to produce than static RAM, it is the predominant form of computer memory used in modern computers.[1].

As we are into an era of green computing, the design of energy efficient IT solutions has become a topic of paramount importance . Recently, the primary objective in chip design has been shifting from achieving highest peak of performance to achieving highest performance-energy effi- ciency.Achieving energy efficiency is important in the design of all sort of processors, such as battery-driven portable devices,desktop or server processors to supercomputer.So it has been the primary aim to reduce the power consumption of the overall system for which the power consumed by the memory is to be minimized since memory is the major dominating portion in every SoC s.So we are examining different SRAM structures on the basis of its data stability and power consumption by analyzing its Signal to Noise mar- gin(SNM) and consumed power during the write operation of different SRAM cell structures and comparing it with the Single Ended Dynamic Feedback 8T cell structure in both 90 nm and 45 nm technology using Cadence Virtuoso tool.

II. SRAM STRUCTURES

An SRAM Cell basically is a cross coupled inverter,which is cyclic in nature,that is one's output is fed as input to the other and so on.So realizing this structure using cmos transistors again reduces the power consumption.A total of four transistors would be enough to implement the basic structure of an SRAM which is a cross coupled inverter. So the extra added components are added for enhancing certain desired features of the system.According to the number of transistors and its alignment there are several SRAM

cell structures.Usually the naming is done according to the number of transistors in the cell.

A. Conventional 6T

An SRAM cell implemented using 4 transistors is modified by adding two more transistors into the structure.The two added transistors are in order to access the bit lines(BL) through which data is read and written;therefore those tran- sistors are known as access transistors. An SRAM cell has three different states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in read mode and write modes should have "readability" and "write stability", respectively. The three different states work as follows: Standby:If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 M4 will continue to reinforce each other as long as they are connected to the supply. In theory, reading

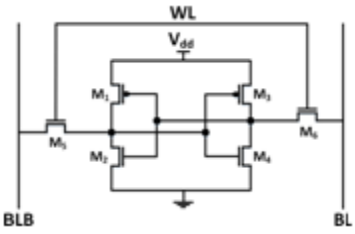

Fig. 1.
Conventional 6T SRAM cell

only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line,
e.g. M6, BL. However, bit lines are relatively long and have large parasitic capacitance. To speed up reading, a more complex process is used in practice: The read cycle is started by precharging both bit lines BL and BL, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical 1 and 0) by an external module (not shown in the figures). Then asserting the word line WL enables both the access transistors M5 and M6, which causes the bit line BL voltage to either slightly drop (bottom NMOS transistor M3 is ON and top PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). If the BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored. The higher the sensitivity of the sense amplifier, the faster the read operation.

The write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they

can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M5 and M6 have to be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently, when one transistor pair (e.g. M3 and M4) is only slightly overridden by the write process, the opposite transistors pair (M1 and M2) gate voltage is also changed. This means that the M1 and M2 transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

B. Read Decoupled 8T

6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation in [2]. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T)] cell which offers read static noise margin (RSNM) comparable with hold static noise margin (HSNM) [2][4].Voltage scaling is one of the most effective techniques for power reduction in digital VLSI design with some limitations like loss of static noise margin (SNM), current fluctuations due to process variations and limitations on the number of cells connected to a single bit-line. In another way researchers have developed several methods for reducing the standby voltage of SRAM cells, so that the circuit can run at an optimum speed and then sleep after completion of the operation to reduce the leakage power consumption.

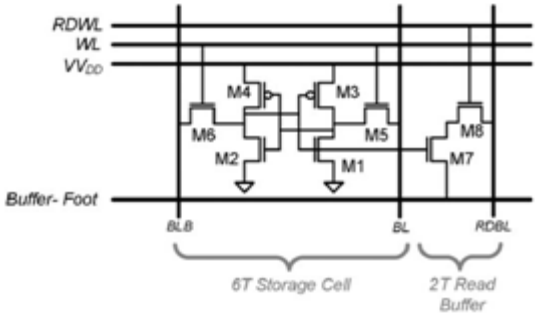

Fig. 2. Read Decoupled 8T

C. 9T SRAM Cell

A 9T SRAM cell shown in figure is used for simulta- neously reducing leakage power and enhancing data stabil- ity.The 9T SRAM completely isolates the data from the bit lines during read operation.The idle 9T SRAM cells are placed into a super cut off sleep mode there by reducing the leakage power consumption.Writing into 9T us initiated by asserting word line WL=1 and keeping RD=0.During read operation WL=1 and RD=1.9T SRAM cell is stable during read operation,consumes very less power.The upper sub-circuit of the newq memory cell is essentially a 6T SRAM cell.The lower sub-circuit of the cell is composed of the bit-line access transistors(M7 and M8) and the read

access transistor (M9).The operations of M7 and M8 are controlled by the data stored in the cell.M9 is controlled by a separate read signal.

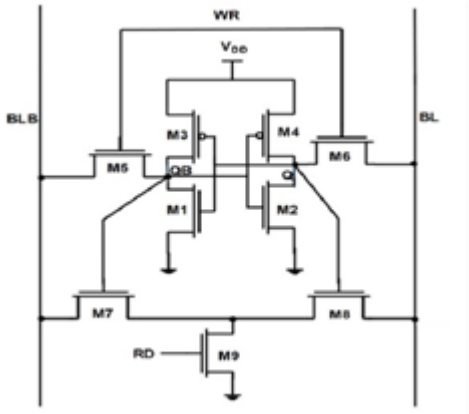

Fig. 3. Read Decoupled 8T

III. SINGLE ENDED DYNAMIC FEEDBACK CONTROL 8T SRAM CELL

To make a cell stable in all operations, single-ended with dynamic feedback control (SE-DFC) cell is presented in Fig.4.[1] The single-ended design is used to reduce the differential switching power during read and write operation. The power consumed during switching of data on single bit line is lesser than that on differential bit-lines. The SE-DFC enables writing through single nMOS in 8T. It also separates the read and write path and exhibits read decoupling. The structural change of cell is considered to enhance the immunity against the processvoltagetemperature variations. It improves the static noise margin (SNM) of 8T cell in subthreshold operations. The proposed 8T has one cross-coupled inverter pair, in which each inverter is made up of three transistors.[11] These two stacked cross-coupled inverters: M1M2M4 and M8M6M5 retain the data during hold modeof the operation . The write word line (WWL) controls only one nMOS transistor M7, used to transfer the data from single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals: FCS1 and FCS2 lines are used to control the feedback cutting transistors: M6 and M2, respectively.

A. Write Operation

The feedback cutting scheme is used to write into 8T cell. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6 transistor. When the RWL is made low and FCS2 high, M2 transistor conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. More- over, when Q changes its state from 0 to 1, the inverter (M1 M2M4) changes the state of QB from 1 to 0. To write a 0

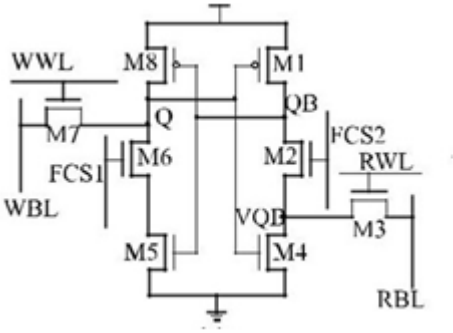

Fig. 4. Single Ended Dynamic Feedback Control SRAM Cell

at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up pMOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other.

B. Read Operation

The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation (Table II), therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operation, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output.

IV. POWER AND SNM

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS

devices are best known for low power consumption.CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency,dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption. The static noise margin (SNM) is the maximum amount of noise voltage VN that can be tolerated at the both inputs of the cross-coupled inverters in different directions while inverters still maintain bi-stable

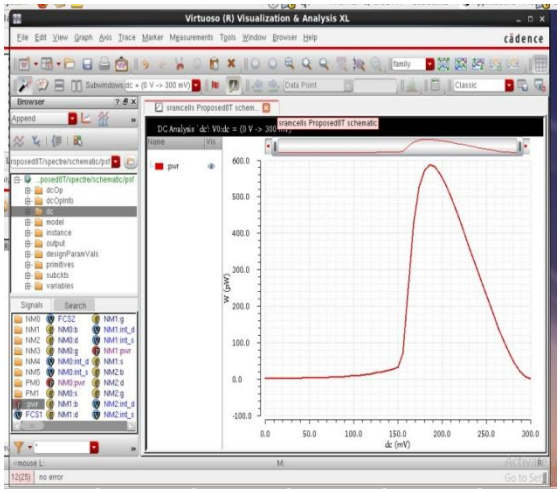

Fig. 5. Power obtained for SEDFC 8T SRAM cell at VDD=300mv

operating points and cell retains its data [5]. In other words, the static noise margin (SNM) quantifies the amount of noise voltage VN required at the storage nodes of SRAM to flip the cell data.

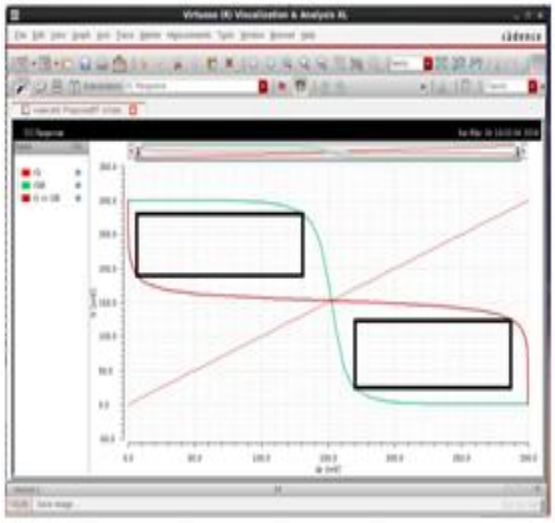

Fig. 6. Butterfly curve for SEDFC 8T SRAM Cell at VDD=300 mv

TABLE I

POWER OBTAINED FOR DIFFERENT SRAM CELL STRUCTURES AT 45 NM TECHNOLOGY

V. RESULT

VDD	6T	RD 8T	9T	SEDFC 8T
300 mV	0.97 nw	0.69 nw	1.4 nw	0.59 nw
2 V	245.4 uw	296.4 uw	272 uw	116
RFID	Mediu m	High	High	

VII. CONCLUSION

The static Random Acces Meomry continues to be a critical component across wide range of microelectronics applications from consumer wireless to high end workstation and microprocessor applications.It provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAM s in systems that require very low power consumption. Another driving force for SRAM technology is low power applications.Standby power of SRAM memories is very low inspite of high density of transistors.SRAM cells

TABLE II

SNM OBTAINED FOR DIFFERENT SRAM CELL STRUCTURES AT 45 NM TECHNOLOGY

VI. RESULT

VDD	6T	RD 8T	9T	SEDFC 8T
300 mV	106m v	105m v	90 mv	118 mv
2 V	0.5 V	0.6	0.6	0.65

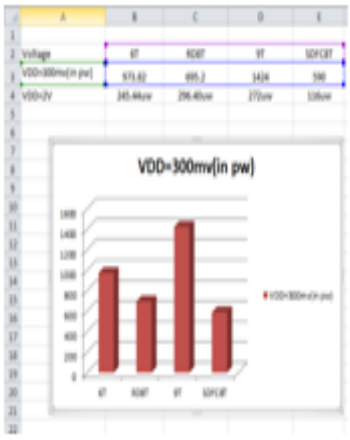

Fig. 7. Graphical analysis of power obtained for diffrent SRAM structures

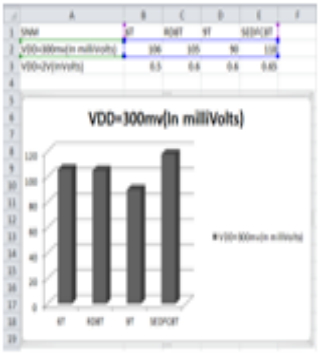

Fig. 8. Graphical analysis of SNM obtained for different structures

have high noise immunity due to larger noise margins, and have ability to operate at lower power supplies .In this study a detailed analysis, evaluation and discussion on three different cell structures in comparison with a SEDFC 8T cell structure was carried out.From the study the SEDFC 8T cell resulted as the lowest power consuming cell both in 45 nm and 90 nm technology.The single ended arrangement and feedback control signals reduced the overall power consumption of the circuit. The SNM was also found to be better experienced in SEDFC 8T cell in comparison with the others.

VIII. ACKNOWLEDGEMENTS

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