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# Effect of Dielectric Constant on Different Capacitance in Interconnect for 10nm Technology for ULSI Circuit

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***Abstract*****—** Our work is to analysis the various interconnects capacitance for 10 nm technology nodes. In this work the line to ground, line to line and crossover capacitance were determined for different dielectric materials. Thereafter the variation of interconnect capacitance over an interconnects dimension were analyzed in details. In this paper we estimated the different capacitances which are form between interconnect using the mathematical approach through Matrix laboratory (MATLAB) software. This step is necessary to calculated for reducing the RC delay time of the IC. RC delay reduces device area and enhances the operation speed of the Integrated circuit. The present work will be helpful for future nanotechnology node in Ultra large scale integration(ULSI) circuit.

Keywords- *interconnect capacitance, low-k materials, BEOL.*

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## 1. Introduction:

Continuous reduction in interconnects dimensions leads to high density of electronic circuits on a single chip. Integration of such lots of circuits on single chips leads to a manufacturing of a small size, high speed and low power semiconductor devices. But on the other hand this high packing density causes many serious issues like RC delay, power consumption, crosses over distension at back end of line (BEOL). Such issues becomes a breaker to further reduce the device size[1-2]. Also to interconnect the increasing number of devices on single chip a number of metal layer also needs to be increases. But the reduction in metal layer dimensions increase resistance of interconnect and leads to increase the RC delay. [3] The reduction in device size beyond a certain layer need for searching new materials like lower dielectric constant material and metal for future technology [4]. in order to overcome aforesaid issues. As per ITRS the material with ultra-low-k dielectric constant are in great demand as a interlayer dielectric layer (ILD).Lots of research is reported based on experimental level. The size of devices reduced towards nano region hence the small variation in device dimensions causes the significantly change in electrical properties[5]. As the complexity of devices increases radically with 10 nm technology there very need to compute its parasitic components mainly metal wiring capacitance accurately. Such study will helpful to replace the conventional materials with new materials. But their valuation is compiles and required lots of work, Interconnect and the device performance are very much interlinked and hence, it is essential to investigate the capacitances involved in device performance. The interlayer dielectric has been a bottleneck for the efficient performance of the devices. The parasitic capacitance is very vital and has a high impact on device and circuit performance. The parasitic capacitance makes significant distortion in device and de-grades its performance, while the spacer dielectric material drastically influence to the fringing capacitance. Thus the details and accurate estimation and analysis of various capacitance formed in interconnect is highly needed. In present work the various capacitances were estimation for 10 nm technology node using the model reported by Kurokawa et al[6].

## 2. Literature survey

Bhavana Joshi and her group analyzed the interconnect capacitance for 32nm technology using the low dielectric material. Trong Huynh-Bao etal reported analysis of the interplay between transistors and interconnect delay and the variability induced by back-end-offline (BEOL) process. Ruth Brain studied the relative comparison of interconnect and transistor scaling and key interconnect scaling challenges. Mikhail R. Baklanov et al reported the review on different low-k material for advanced interconnects.

## 3. Mathematical approach

Continuously reducing device size causes the interconnect issues due to spacing between two interconnect form various capacitance. Such capacitance resulted to the further change in device electrical parameters. Thus formation of capacitance in BEOL i.e in interconnect is very essential for further reduction in device size. The capacitance can be calculated using the different numerical formulas. Structure of interconnect geometry with two ground plane is presented in figure 1.

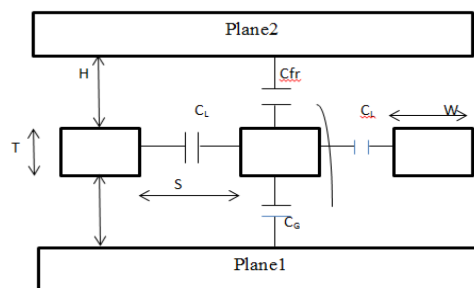


**Figure 1: Interconnect structure between two ground planes[8].**

Figure clearly showing the different formation of capacitance such as line to line (coupling/lateral capacitance) ,line to ground (Overlap capacitance) and crossover capacitance (fringe capacitance) between different metal lines. The coupling capacitance is the capacitance between parallel interconnect edges of two metal lines in same plane. The

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capacitance be-tween the edge of one metal and surface area of other metal above or below the first metal is called as crossover or fringe capacitance, whereas the parallel plate capacitance or the capacitance between surfaces of two metals is known as overlap capacitance. As shown in figure a thin layer called as Interlayer Dielectric was used for the separation for metal lines. The ILD layers play important roles in order to control the RC delay of the circuits in ULSI circuits. Thus we focused the present paper on the variation of different interconnect with metal dimension. Along with this the variation capacitance by using different dielectric material were also studied. The paper presents the of detail analysis of overlap, crossover capacitances with variation in metal wire width, wire spacing and wire thickness. Also the dependence of capacitance on dielectric constant of ILD materials is also studied in details in present paper.

The equations involved in the analysis of these capacitances are given below. For all the simulation work for different low dielectric constant like (k = 3.8, k=2.4, k=1.2) value for calculating the different capacitances[7]. In present paper for proper analysis of interconnect capacitance over the variation of device dimensions we used a numerical method in MOS structure.

### 3.1. Line to ground capacitance (Overlap capacitance)

The interconnect capacitance is playing very important and has significant effect on device electrical performance. Thereafter the capacitance formed in BEOL causes the degradation of device performance. In addition to the the ILD material used for separation metal wire also highly influence to the fringing capacitance. Thus to overawed the issues the interconnect structure should be advanced. The reduction in device dimension leads to the lowering the interconnect parameter's such as width and thickness. Such change in parameters raises the devices time delay. It is very necessary to note that the high aspect ratio is imperative in metal to ground capacitance which is directly proportional to line width and material dielectric constant has observed from the following equation. The line to ground capacitance can be calculated by using following equation-1 [5-6].

$$C_0 = \epsilon\left(\frac{W}{H} + 1.086\left(1 + 0.685\, e^{-T/1.343S} - 0.9964\, e^{-S/1.421H}\right)\right)$$

………..(1)

### 3.2. Line to line capacitance (coupling/lateral capacitance)

It is obligatory to investigate coupling capacitance, as for the high aspect ratio and the increased line thickness increases delay in the device and creates high signal coupling noises. These limitations will hamper to the practical implementation of scaling techniques. Thus, replacement of conventional ILD material with low dielectric material effectively reduces interconnects parasitic capacitances which lead to further lowering the RC delay and crosstalk effect. The equation 2 is used for the determination of line to line capacitance.

$$C_L = \varepsilon\left(\begin{array}{c} \frac{T}{S}\left(1 - 1.879e^{\frac{-H}{0.31S}} - \frac{-T}{2.474S} + 1.302e^{\frac{-H}{0.082S}} - 0.1292e^{\frac{-T}{1.326S}}\right) \\ +1.722\left(1 - 0.654e^{\frac{-W}{0.3477H}}\right)e^{\frac{-S}{0.651H}} \end{array}\right)$$

……………(2)

### 3.3 Crossover Capacitance

Such type of capacitance is formed in three adjacent metal layers. The total capacitance on a wire passing many crossings can then be easily determined by combining the crossover capacitance with the two-dimensional (2-D). The crossover capacitance can be determined using following equation-3.

$$C_C = \varepsilon\left(\begin{array}{c} \frac{W_1W_2}{H} + 0.9413\left(1 - 0.326e^{\frac{-T_1}{0.1335T}} - 0.959e^{\frac{-S_1}{1.986H}}\right)2W_2\left(\frac{S_1}{S_1+0.01H}\right)^{0.2} \\ +0.9413\left(1 - 0.326e^{\frac{-T_2}{0.1335_2}} - 0.950e^{\frac{-S_2}{1.986H}}\right)2W_1\left(\frac{S_2}{S_2+0.01H}\right)^{0.2} \\ +1.14\left(1 - 0.326e^{\frac{-T_1}{0.1335_1}} - 0.959e^{\frac{-S_1}{1.986H}}\right)(S_2S_1)^{0.5}\left(\frac{W_2}{H}\right)^{0.182} \\ +1.14\left(1 - 0.326e^{\frac{-T_2}{0.1335_2}} - 0.959^{\frac{-S_2}{1.986H}}\right)(S_1S_2)^{0.5}\left(\frac{W_1}{H}\right)^{0.182} \end{array}\right)$$

……..(3)

Where, the $C_O$ is the overlap capacitance, $C_L$ is line to line capacitance, $C_C$ is crossover capacitance, e is dielectric constant, W is width of interconnect, T is thickness of interconnect, S is spacing between two interconnects in plane, H is thickness of dielectric. The total capacitance $C_T$ is determined by adding the $C_O$, $C_L$, $C_C$ for respective planes.

## 4.Results and discussions:

### 4.1 Cross over capacitance:

The crossover capacitance is the capacitance from between two metal wire. Thus the variation of space between two metal wire and metal wire width leads to the significant effects on capacitance. The three dimensional plots for capacitance variation with metal wire width and spacing between two metal wires with different colours shades in shown in figure 2.

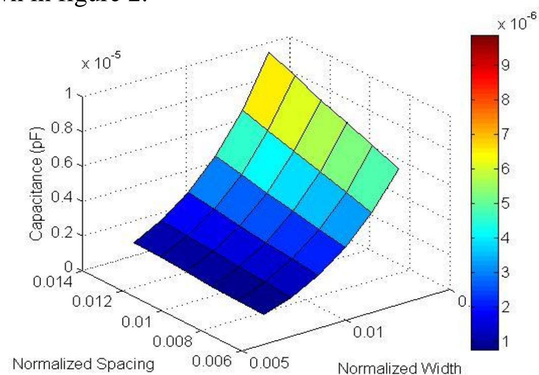


Figure2 Variation of capacitance Vs. interconnect Space and width for (a) K=3.8

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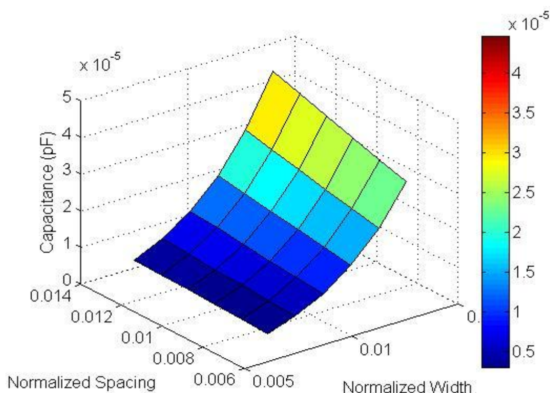


Figure 2 Variation of capacitance Vs interconnect Space and width for(b) k=2.4

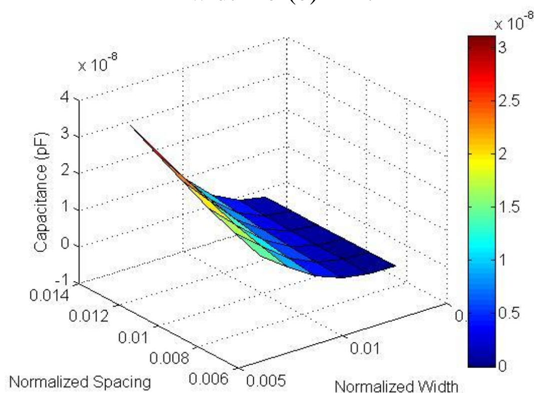


Figure 2 (c) Variation of capacitance Vs interconnect Space and Width for K=1.2

From figure, the capacitance is found to be decreases with reduction in wire width and space. From figure 2 (a) and (b) , it is observed that the overlap capacitance decreases from 0.1631 to 0.0113pF and from 0.3605 to 0.0282 pF from the dielectric constant of 3.8 and 2.4. Also for k=1.2 shows opposite effect it shows the increase in capacitance**.** Thus from figure it reveals that the dielectric constant also plays an important role for variation in capacitance.

**4.2Line to Ground capacitance (Overlap capacitance) :**

Figure3 illustrated the Variation of line to ground capacitance i.e overlap capacitance with space between two wire and wire width. Also in addition to this the effect of ILD material dielectric constant on the overlap capacitance is also studied.

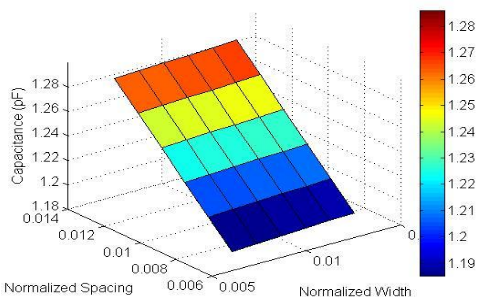


Figure 3(a) Overlap capacitance vs interconnect Space for k=3.8

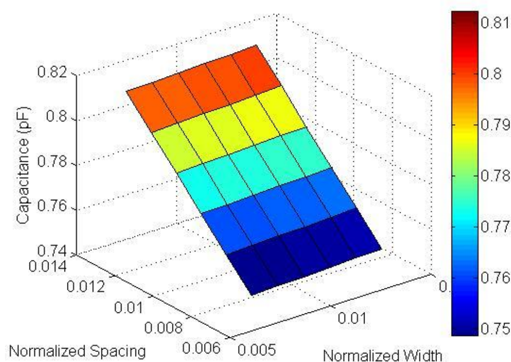


Figure 3(b) Overlap capacitance vs interconnect Space for k=2.4

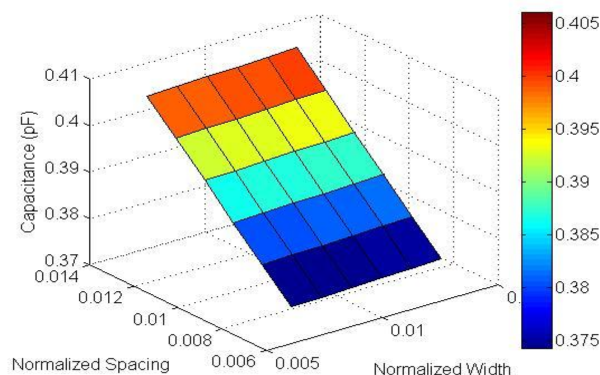


Figure 3 (c) Overlap capacitance vs interconnect Space and width for K=1.2

**4.3 Line To Line Capacitance (Coupling capacitance):**

The investigation of line to line capacitance i.e coupling or lateral capacitance dependence on spacing between the two metal lines has been carried out as shown in figure 4.Figure shows the nonlinear variation of capacitance.

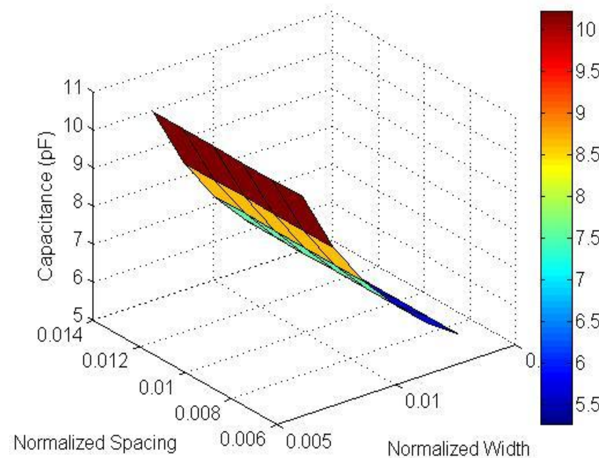


Figure 4 : Line to Line capacitance for a) K=3.8

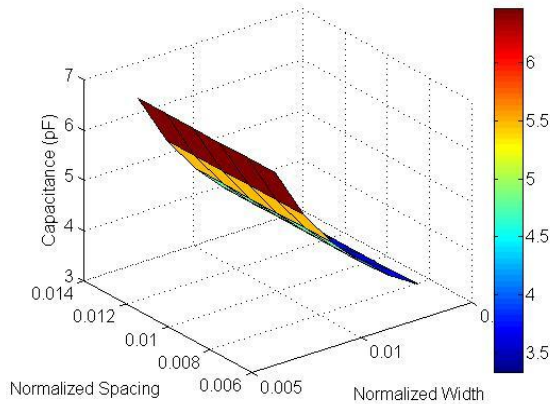


Figure 4 : Line to Line capacitance for b) for 2.4

From figure it reveals that as decrease in wire width the capacitance was found to be increasing. From figure 4 (a) decrease in width from 0.014nm to 0.005 the capacitance found to be increase from 1 to 11pf for k=3.8. Also from figure 4(b) the capacitance found to be increased to 7pf for k-2.4.

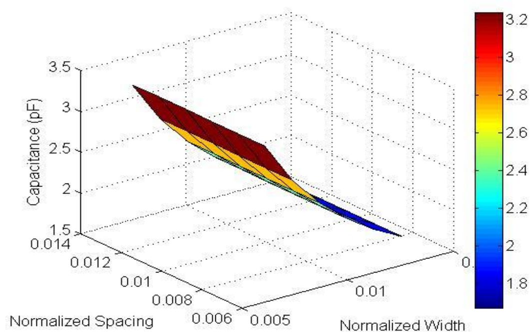


Figure 4(c): Line to Line capacitance for k=1.2

Also as shown in figure 4(c) the capacitance was found to be increase to 3.5pf with decrease in wire width. But on the other hand it is observed that as decrease in dielectric constant of the ILD material the capacitance is found to be decrease. It is found that the capacitance was found to be decreased from 11pf to 3.5pf with decrease in k value from 3.8 to 1.2. This suggests that the capacitance can be controlled by decreasing the k value. The decrement in capacitance leads to the reducing the RC delay. Thus RC delays is decreased by replacing the conventional ILD material with lowest dielectric constant

## 5.Conclusion:

In present paper the estimation of different capacitance such as crossover, coupling and overlap capacitance formed in BEOL interconnect structure was analysed succesfully in details. The capacitances were determined by using mathematical approach. The work was carried out for 10nm technology node. The analysis of variation of capacitance with the variation in wire width, space between two metal line and thickness was carried out details. Further the work was extended to study the effect of ILD material k value on the estimated interconnect capacitance. In present work it is illustrated that the variation in interconnect parameters like space between two wire, wire thickness and width shows a significant change in capacitance. In addition to this, the work extended to study the ILD material k value effect on capacitance. This study clearly shows that the decrement in k value decreases the capacitance. Thus by selecting proper value of k value can helps to controlled capacitance. Thus from this study it is reveals that dielectric constant plays an important role in controlling RC delay of ULSI circuit. From the work it is reveals that the capacitance was very sensitive to the metal width, thickness and space and thus this work will very helpful for future nanoelectronics in ULSI circuit.

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