# Low Power and Delay Efficient 32 –Bit Hybrid Carry skip Adder Implementation using HDL

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***Abstract*****—**The Carry skip adder (CSKA) is an efficient adder in terms of power consumption and area usage as the critical path delay and power-delay product of CSKA is small compared to other conventional adders. However the use of Multiplexer of Carry skip logic in CSKA causes an increase in power consumption due to the use of large numbers of Transistors (i.e., 12). Hence, a power efficient CSKA called Concatenation-Incrementation (CI-CSKA) has been proposed. In CI-CSKA, the power reduction can be enhanced by replacing the Multiplexer that is used to skip the carry with Or-And-Invert (OAI)/And-Or Invert (AOI) logic. As the number of transistors is reduced to half by using AOI/OAI logic when compare to MUX, Power reduction is achieved without compromising the speed making it suitable for a wide range of low power applications. For further improvement in delay, hybrid variable CICSKA has been proposed. Here the size of each stage is varied with increment in size from stage1 to nucleus stage and then decrement to the final stage. Simulations by using hybrid variable latency CSKA produces a high speed and reduce the power consumption. By using a hybrid variable latency technique (which uses parallel prefix network) will further reduce the power consumption when compared to the simple variable stage style implementation. The entire architecture can be modelled using Verilog code with the help of Xilinx ISE tool. The efficiency of the proposed structure for variable stage style was studied by comparing their power and delay with those Conv-CSKA,CICSKA.

***Keywords***- *Carry skip adder (CSKA),Low Power, Delay Optimization.*

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## I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.Although adders can be constructed for many number representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require more logic around the basic adder.There are many adderfamilies with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA),carry increment adder (CIA), carry skip adder (CSKA), carryselect adder (CSLA), and parallel prefix adders (PPAs).The RCA has the simplest structure with the smallest area and power consumption, but with the worst critical path delay.In the CSLA, the speed, power consumption, and area usagesare considerably larger than those of the RCA.

Addition is the most basic arithmetic operation and it plays a vital role in filter designs, processors and DSP applications. Now-a-days, adders are mostly used in the microprocessor designs and Digital Signal Processing-chips. Adders are essential not only for addition, but also for subtraction, multiplication, and division. A fast and accurate operation of the digital system is greatly influenced by the performance of the high speed adders. In VLSI industry, power and delay are the performance parameters that shows adverse effect on any design.So,we have to design the architecture in such a way that it should have low power,should occupy less area and should get the result in less time(i.e., should have the less delay).Now-a-days there is an increase in demand for portable equipments such as cellular phones and notebook personal computer,so there is a need of using area and power efficient VLSI circuits. Low-power and high-speed adder cells have wide range of applications for instance, battery operation based devices.Now the challenge is to design the adder with less power consumption maintaining the high performance in different types of circuits.Until now, the power consumption has not been a big deal because of the availability of large packages and other cooling techniques in wide ranges and they have the capability of dissipating the generated heat.But increasing density in addition to the size of the chips and systems may cause the difficulty in providing adequate cooling.So, this will add either add significant cost to the system or provide a limit on the amount of the functionality that can be provided. So, additional equipment (i.e.,cooling techniques) cannot be used in all the applications because it leads to the increase in the area occupancy of a circuit.

## II. PREVIOUS WORK

The Conv-CSKA consists of stages in which each stage contains chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The Multiplexer is used to skip the carry to next stage.In case of RCA,the worst case delay occurs when the two N-bit numbers are in propagate mode.The delay for an N-bit RCA can be calculated by the following mathematical expression

$$T = (n-1)t_c + t_s$$

Where ts is the delay used to compute the sum of the last stage and tc is the delay through the carry stage of a different FA.The major drawback in it is carryin for the present stage is obtained only after the carry produced from the previous stage.But due to its excellent advantage in simplest architecture it cannot be replaced,so a modified structure in RCA known as carry skip adder was designed. The architecture of Conv-CSKA is as follows;

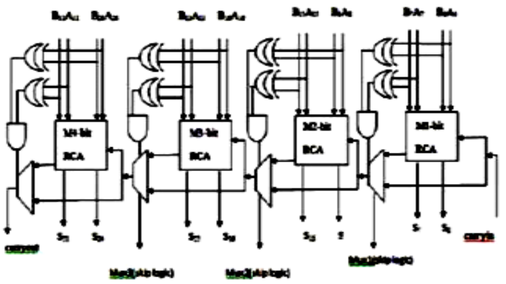

**Figure1.Architecture of Conv-CSKA**

In Conv-CSKA structure, the main target is to reduce the delay by modifying its implementation based on the static CMOS design. The modification increases the speed with area and power consumption comparable to that of RCA.

$$P_i = A_i \oplus B_i, i = 1,2.......N$$

Where Pi is the propagation related to Ai and Bi. Therefore, it shows that the delay of RCA is linearly related to N. In the case, where cascaded FAs are in the propagated mode, the carry output of the chain is equal to the carry input. The carry skip logic in CSKA detects this situation. It doesn't wait for the operation of FA chain to be completed and it makes the carry ready for the next stage. The skip operation is performed by using the multiplexer and gates as shown in the figure. Based on the explanation, in CSKA the N FAs are grouped in Q stages. Each stage contains one RCA block with a skip logic, and Mj FAs(8) where j=1,…..,Q.(=4)[Totally 4 stages(8 FAs at each stage),32-bit adder].The conventional structure of the CSKA consists of stages that contains chain of 2:1 multiplexer (carry skip logic) and FAs. Through 2:1 multiplexer RCA blocks are connected to each other which can be used in one or more level structures. In each stage the input of the multiplexer (skip logic) is the carry input of the stage and the output of its RCA block (FA chain) is the carry output. The product of the stage is used as a selector signal of the multiplexer. The CSKA is implemented by using Fixed Stage Size (FSS) and Variable Stage Size (VSS). The highest speed is obtained from the VSS structure. For the implementation of skip logic MUX is used which requires 12 transistors for its implementation.This leads to the hardware complexity.So,MUX used in skip logic was replaced by AOI,OAI gates, which requires only 6 transistors.Hence,there is a 50 % decrement in area usage and power consumption.The structure whose skip logic contains AOI,OAI gates is named as CICSKA(Concatenation and Incrementation Carry Skip Adder).. The architecture of CI-CSKA is as follows;

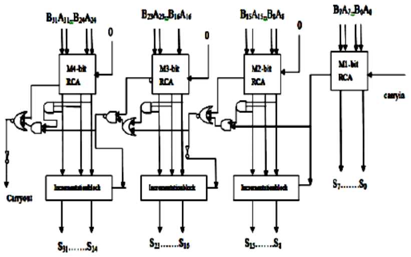

**Figure2.Architecture of CI-CSKA**

## II.A DELAY OF THE PROPOSED STRUCTURE

The use of static AOI and OAI gates, which requires six transistors for the implementation leads to decrement in the area .This further reduces the delay.Except for the first RCA block all the inputs for the remaining RCA blocks are given as zero(i.e.,carryin) hence the name concatenated.The obtained intermediate result is given to incrementation block to get the final SUM. The critical path of the proposed structure contains three parts,which includes a chain of FAs of first stage,path of the skip logics,incrementation block in the last stage.Hence,the path delay can be expressed as,

$T_{AND}$ and $T_{XOR}$ are the delays of inputs AND and XOR gates.The delay of the skip logic depends on the average of delays of AOI and OAI gates.

$$T_D = [M_1 T_{CARRY}] + [(Q-2)T_{SKIP}] + [(M_Q - 1)T_{AND} + T_{XOR}]$$

$$T_D = [M_1 T_{CARRY}] + \left[ (Q-2)\left( \frac{T_{AOI} + T_{OAI}}{2} \right) \right] + [(M_Q - 1)T_{AND} + T_{XOR}]$$

$T_{AOI}, T_{OAI}$ are the delays of AOI and OAI gates.

## II.B. CALCULATION OF STAGE SIZES

The size of each stage can be obtained by the following expression

$$M_{opt} = \sqrt{\frac{N(T_{AOI} + T_{OAI})}{2(T_{CARRY} + T_{AND})}}$$

## III. PROPOSED VARIABLE HYBRID CI-CSKA

In variable hybrid CI-CSKA to have further decrement in delay the size of each stage is varied(i.e., number of RCAs in each block).The number of RCAs in each block were increased up to the nucleus stage(stage with larger size),from there, thenumber of RCAs in each block were decreased.The stage with larger size is implemented with brent kung adder since it has good compromise between delay and power consumption. The architecture of variable Hybrid CI-CSKA is shown in the following figure,

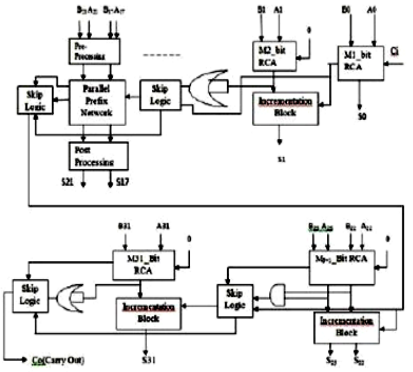

**Figure3:Architecture of Variable HybridCI-CSKA**

In variable hybrid CSKA structure, the size of eachstage is varied by considering the following steps:

1) The size of the first stage is one(i.e., number of FAs in RCA block is one).

2)Based on the delay of product of sum of its RCA block and delay of carry output of present stage the size of the next stage is determined.So,from the second stage to nucleus stage the size of the RCA block (i.e.,number of FAs in each RCA block)gradually increases.

3)The above step is repeated until the summation of all the sizes up to the nucleus stage becomes larger than N/2(where N is the size of the adder).

4) After the nucleus stage to the last stage, the size of the stage is determined based on the delay of incrementation block of present and previous stages and delay of skip logic. The design of a carry skip adder is based on the definition of propagate and generate signals and is mathematically expressed as follows:

$$P_i = A_i \oplus B_i,$$
$$G_i = A_i \bullet B_i$$

Where is the propagate signal and is the generate signals,and are the input bits.The carryout from the i^th stage(carry input to (i+1)^th stage) is expressed as

$$C_{i+1} = G_i + P_i C_i$$

The architecture of Brent kung Adder is as follows:

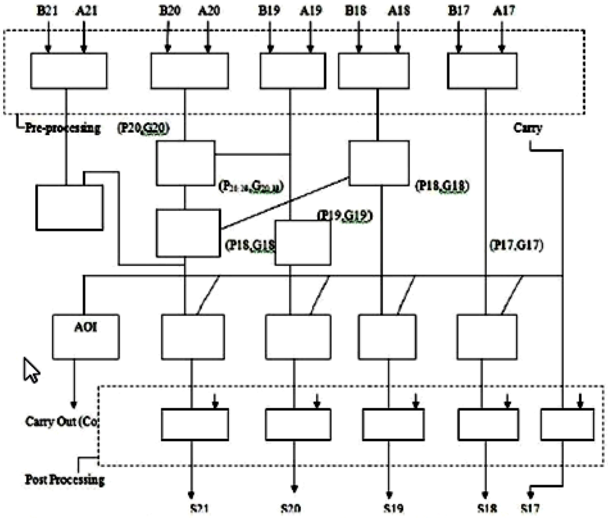

**Figure4:Architecture of Brent Kung Adder**

As shown in the figure4,in the pre-processing level,propagate and generate signals are calculated from the input bits and is as shown in Fig4.In the second level Brent Kung adder is used to calculate the longest carry,this was generated ahead when compared to any other intermediate signal.For a 5-bit adder if normal RCA is used carry is generated after five stages,but in case of Brent Kung adder Carryout is obtained after three levels[13] so,delay is further more reduced.In the third level i.e.,postprocessing level, the output sums are calculated.

## IV. Results and Discussion

When compared to CONV-CSKA there is 50% decrement in the delay in CI-CSKA.By varying the sizes of stages delay can further be decremented. By replacing MUX with AOI and OAI gates area reduced to 50% there by decrease in the 50% delay.By varying the sizes of each stage there is further decrement in delay.In Conv-CSKA use of 2:1 multiplexers for the skip logic causes more delay and area since it requires 12 transistors to implement.So,in the CI-CSKA technique these 2:1 multiplexers got replaced by AOI,OAI gates which requires only 6 transistors to implement causing a decrement in area,power,delay.In CI-CSKA delay is reduced to 50% when compared with the Conv-CSKA.By varying the sizes of each stage in Variable Hybrid CSKA with Brent Kung Adder in the nucleus stage all the performance parameters were improved.

Table1.Delay comparision of Conv-CSKA,CI- CSKA, Variable Hybrid CSKA

| Structure | Delay |
|---|---|
| Conv-CSKA | 46.472ns |
| CI-CSKA | 29.056ns |
| Variable Hybrid CSKA | 20.52ns |

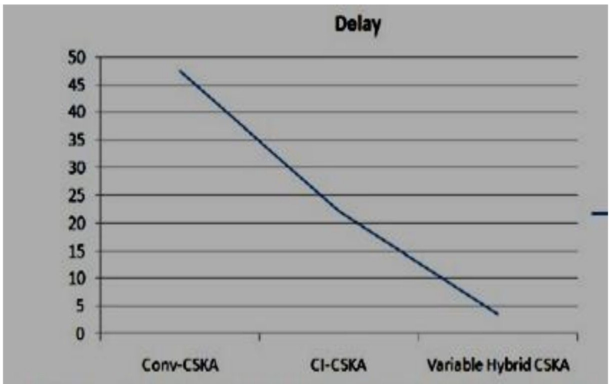

**Figure 5.Delay comparision for Conv-CSKA,CI-CSKA,Variable Hybrid CSKA**

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