

Design and Implementation of High speed and Energy Efficient MAC using Adaptive Logic

S. S. L. Ch. Mounika

Department of Electronics and Communication
Engineering
UCEK, JNTU Kakinada
Kakinada, Andhra Pradesh, India
E-mail Id: mounikasarella@gmail.com

Dr. K. Babulu

Department of Electronics and Communication Engineering
UCEK, JNTU Kakinada
Kakinada, Andhra Pradesh, India
Email Id: kapbbl@gmail.com

Abstract: Every digital circuit objective is to achieve MEP system i.e., minimum energy, minimum power, minimum voltage. These constraints can be achieved through adaptive logic. Adaptive logic is one of the fastest and innovative logic that has been implemented in digital circuit. Adaptive logic is implemented using the combination of both Nano magnetic technology and CMOS technology. Adaptive technique works very effectively in both threshold and sub – threshold regions. Internet - of - Things (IoT) is on the threshold of a massive breakthrough. Timing-error-detection (TED)-based systems have been shown to reduce power consumption or increase yield due to reduced margins. Reducing voltage in the circuit results in slow operation that incurs more delay. Canary circuit have been designed for error detection and error correction approach. Canary circuit results in large delay. Adaptive logic have been designed with dual latch phase in each stage. A combination of XNOR gate and flip-flop around each stage is added for the verification of correct operation. The entire architecture was modelled using Verilog code with the help of XILINX ISE tool.

Key words: Timing margin, TED (TimingErrorDetection), TEP(Timing Error Prevention), canary circuit

I. INTRODUCTION

Energy efficiency has emerged as a critical design requirement. In order to obtain the maximum power savings it is essential to scale the supply voltage as low as possible while ensuring the correct operation of the system. Maximum possible supply voltage based on the potential of the circuit, produces better results in correct operation. Means if there is insufficient voltage to the circuit the process of operation will be slow so if we give less voltage means lag will be performed in the circuit that produces delay. Many energy efficient design techniques have been proposed in an efficient way of reducing energy consumption. Reducing voltage in the circuit results in slow operation that incurs more delay several techniques such as pipelining, parallel processing have been proposed to allow large reduction in voltage. These techniques are overcome by using timing margin technique. This is explained in brief in section I.

The rest of the paper described as section II deal with background, section III deals with basic traditional circuit connected to digital circuit section IV deals with adaptive logic connected to digital circuit and section V describes the results and followed by a conclusion.

II. BACK GROUND

A major challenge in Timing margin [3], [4] technique reduction methodologies has increased the timing error probability variations. Variations are divided into two types 1. Spatial variation, 2. Temporal variation Transistors are effected by spatial variation. Spatial variation is divided into

two type's 1.Global variation, 2.local variation. Electrical characteristics of the devices effects global variation. Transistor characteristics in more unpredictable way due to randomness effects local variation. Temporal variations are divided into two type's 1.static variation 2. Temporal variation. During fabrication period which effects the static variation. Due to environmental changes, such as temperature, supply voltage noise, and aging cause the transistors to experience variability depending on time which effects temporal variation. To accommodate the potential increase in circuit delay caused by the variations more timing margin is given in traditional design approaches. To overcome the limitations in the traditional design there are two approaches to reduce the error in the current circuit that incurs delay in the circuit. One is to predict the occurrence of errors to avoid timing violation (error prediction approach), and the other is to detect actual errors and correct them (error detection approach). There are many error correction methods among them instruction replay and counter flow pipelining are time consuming techniques which are best known error correction techniques though they incurs the circuit with more delay. In instruction replay if an error occurs at a particular stage, it allows the cycle to propagate

until the last stage, and then all stages in the pipeline are in embarrassment state. If there are N pipeline stages, this will require N cycles. The failed instruction is then reissued to the pipeline, with the clock. This rerun takes 2N cycles, and so the completion time of the next instruction that follows the error is delayed by 3N cycles. The counter flow pipelining technique is a error detects an error in the entire pipeline if an error is generated in the particular stage it will be corrected in the next state from then new instructions are reissued starting from the next cycle.

(a) Timing Error Detection (TED)

Key component of TED [5] is EDS (Timing Error Detection). EDS circuit generates error signals when path fails. This is also called as late signal detection concept a well-known synchronization concept. If there occurs an error in order to reduce the error EDS circuit is composed by using sequential and combinational circuits that are placed in the critical logic circuit to reduce the error which automatically reduces the delay. In EDS circuit timing error is flagged off to the circuit when the data is transmitted to the logical circuit this delay is reduced by using EXOR gate. Where the inputs are given to it from the output of combinational and sequential elements. Thus, the minimum delay for the combinational logic is the TED window which is composed by using EDS circuit.

(b) Timing Error Prevention (TEP)

We combine TED with TB (Time Borrowing) which results in TEP. Combining TED with TB into TEP conceives system can tolerate late coming signals without the requirement of additional components, which follow the timing margin technique. This method works as follows When a late signal arrives, TB occurs normally. TB events are detected with EDS latches. TB borrows the time from previous stage. TB is nothing but latch. Latch is generally used for time borrowing concept. Latch will have enable signal. In latch when enable signal is high it is called transparent latch. The processing speed of the transparent latch is high compared to normal latch. Normal latch (when enable signal is low i.e., 0) Transparent latch (when enable signal is high i.e., 1). With TEP, the maximum amount of borrowed time is the latch transparent time. Thus, recovery is necessary to prevent borrowed time to accumulate beyond this limit. Late signals are allowed for both TED and TEP. When TEP is integrated using dual latch nothing but using 2 latches in the single stage. Resulting system cannot only tolerate late signals, but does not require

Additional hold buffers on fast paths. This is a large advantage compared with a traditional TED system. This is discussed in brief in section IV [9].

C) Simplified Power Management for Adaptive Logic

For battery operated systems, generally the battery voltage VBatt decreases as the battery discharges previous designs aims to keep VDD constant over this battery continuously regulates a discharge concept. In order to maintain high efficiency in the circuit this ensures a fixed operating voltage but due to constant voltage battery gets discharge [6]. Above two methods require a complex control circuitry, which leads to a large design.

In order to maintain high efficiency over a large range of VBatt, the Vref must linearly adjust with VBatt. This allows VDD to linearly scale up with changes in VBatt. This provides a nearly constant VDD/VBatt ratio. This allows no fluctuations in the battery. This ratio is called the voltage conversion ratio (VCR) of the dc-dc converter. The ideal VCR, which is n/m, assumes no losses in the converter. The maximum conversion efficiency can be defined in terms of VCR and iVCR

$$\eta_{\max} = \text{VCR}/i\text{VCR} = (m/n) * (\text{VDD}/\text{VBatt}). \text{---(1)}$$

Allowing for a nearly constant VDD/VBatt for changing VBatt enables $\eta_{\max}$ to be achieved for a wide VBatt range. Here technique will be defined as the scaled input regulation (SIR) technique. To provide high efficiency across a large range of VBatt SIR [7] technique is used. In order to avoid constant voltage concept SIR technique is implemented by using a varying voltage concept. This varying voltage requirement can be easily fulfilled by TEP and TED concepts that are used in adaptive logic concept. To obtain MEP (Minimum Energy Point) which is nothing but less voltage, power, delay, error must be achieved in order to achieve MEP. Increasingly large operating VDD range. To employ the traditional approach with variations include by using timing margin technique canary circuit is implemented which is explained in detail in section III.



Fig 1: SC DC-DC Converter

III. BASIC TRADITIONAL APPROACH

To employ the traditional approach with variations include by using timing margin technique canary circuit [2] is implemented There are two error correction circuits namely razor circuit [6] and canary circuit. In razor circuit every stage have main flip-flop and shadow flipflop. These two are provided with a clock of opposite polarity. The shadow flop is always expected to hold correct values even though a timing violation may have occurred in the main flop. Apart from error detection, error correction has also been done. An EXOR gate is used to compare the values of output of the main flop to the shadow flop. In case of a mismatch, timing error is reported and output of the EXOR gate will go high. The output of the EXOR gate is also the select line of the multiplexer which will go high in case of mismatch. During timing violation, instead of taking input from previous stage, the Razor flop [6] will reflect the output of the shadow flop and during the next cycle, correct data will be forwarded to the next stage. Several numbers of stages are included in a single razor circuit which leads a large design. To avoid that drawback canary circuit is been used to detect and correct error in a single stage. This reduces the drawback of razor circuit. The timing error is predicted by comparing the value of the main flop with that of the canary flop. The data input to the canary flop is delayed instead of clock. So the canary flop will run into timing violation before the main flop .An alert signal triggers a warning for possible timing violations. Advantages of canary circuit over razor circuit

1. Elimination of delayed clock
2. Robustness for variations
3. Protection against timing errors

in order to correct the error predefine canary circuit have been introduced to reduce the error in one cycle without introducing any delay in the circuit. Digital circuit is connected to canary circuit

Through CLK. Adaptive logic is implemented by modifying canary circuit for better results which is explained in detail in section IV.

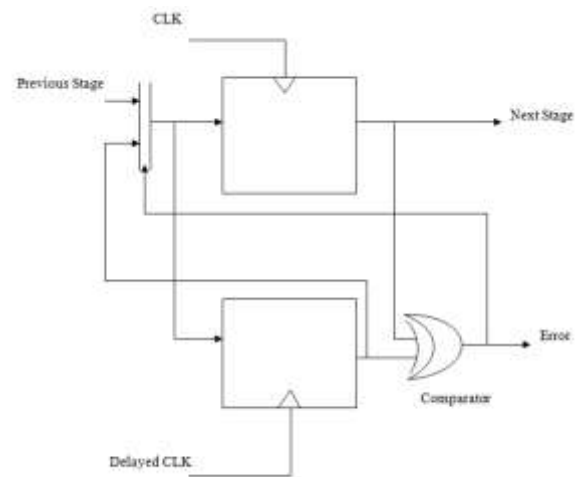


Fig 2: Canary circuit

IV SYSTEM SIMULATION

(a) Adaptive load and Dickson converter

Adaptive logic is nothing but we design a circuit based upon the requirements to result in best output. so here we designed a circuit using canary circuit using dual latch phase at every stage placed at IN and OUT. For varying voltage here we using 3:1 Dickson DC-DC [8] converter to avoid battery discharge concept and to provide variability in voltage. The Dickson SC converter has been shown to provide high efficiency across a large load range TEP load includes dual latch phase provided at both input and output at each stage. Basically usage of latch in the provides less delay by borrowing the time from previous stages if needed. In case any time is been borrowed that will be recovered. The recovery is implemented by using clock control circuit

This is achieved by first combining TB event signals (TBE_NEG[n] and TBE_POS[n]) The clock control circuit latches the aggregated signal at the beginning of the next phase and excludes a single phase out from the external clock (CLK_EXT) in the case of flagged TB event. To avoid glitches, the gating of CLK_EXT is initiated at the middle of the phase using a 90° shifted reference clock (CLK_REF).

A combination of X-OR gate with flip flop around every stage is added for verification of correction operation. Here canary circuit is placed at the end of every stage for error correction and detection purpose as EDS circuit. Circuit can be of any number of stages, we have taken an adaptive circuit with 5 stages for error detection and correction purpose.

(c) Proposed work

Here digital circuit is taken to compare the results between canary circuits and adaptive logic circuit. Clk of digital circuit is connected to adaptive system through CLK_EXT signal. MAC [10] is taken as basic digital circuit to compare the results. In computing, especially digital signal processing, the multiply-accumulate operation is a common

step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is also often called a MAC or a MAC operation

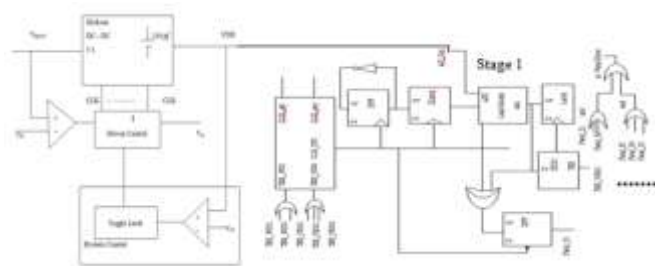


Fig 3: Adaptive test system using canary circuit at the end of each stage

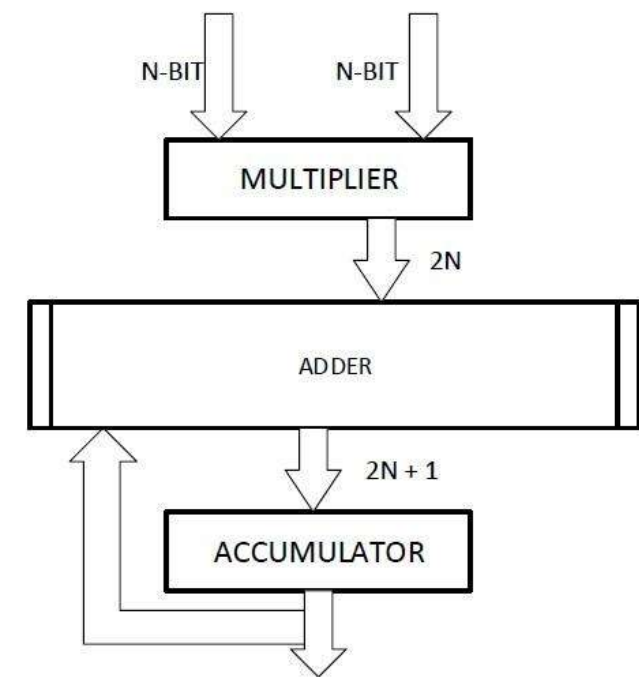


Fig 4:MAC

(c)Simulation Results

The simulation studies involve the delay comparisons of individual 8-bit MAC, 8-bit MAC connected to canary circuit and 8 –bit MAC connected to adaptive system.

8-bit MAC(ns)	8-bit MAC connected to canary circuit(ns)	8-bit MAC connected to adaptive circuit(ns)
4.890	4.458	3.878

TABLE I.Comparison of delay

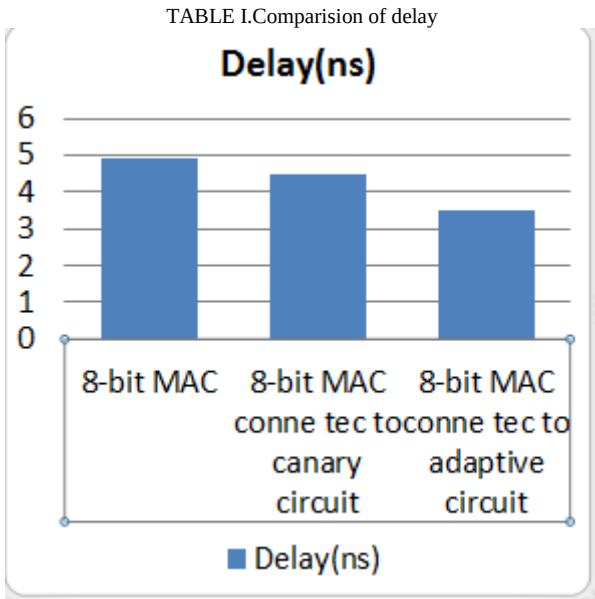


Fig 5.Delay comparison

V Conclusion

Insufficient supply voltage to the circuit causes delay in the circuit and results in incorrect outputs.inorder to supply sufficient voltage SC DC-DC converter is used. Delay is generally caused due to errors, to reduce those errors canary circuit is designed to reduce the errors in single shot without the usage of stages. But by using dual latch phase to the circuit the performance of the circuit is improved than the previous method. By using dual latch phase, canary circuit and a combination of X-OR gate with flip flop around every stage is added for verification of correction operation results in improved output than the previous method.

REFERENCES

[1] IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 24, NO. 4, APRIL 2016 Implementing Minimum-Energy-Point Systems With Adaptive Logic Lauri Koskinen, Member, IEEE, Markus Hiienkari, Student Member, IEEE,Jani Mäkipää, Member, IEEE, and Matthew J. Turnquist, Student Member, IEEE.

[2] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, “Adaptive performance compensation with in-situ timing error predictive sensors for subthreshold circuits,” IEEE Trans. Very Large Scale Integer. (VLSI)

[3] K. A. Bowman et al., “A 45 nm resilient microprocessor core for dynamic variation tolerance,” IEEE J. Solid-State Circuits, vol. 46, no. 1, pp. 194–208, Jan. 2011.

[4] S. Das et al., “RazorII: In situ error detection and correction for PVT and SER tolerance,” IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 32–48, Jan. 2009.

[5] J. Tschanz, K. Bowman, S. Walstra, M. Agostinelli, T. Karnik, and V. De, “Tunable replica circuits and adaptive voltage-frequency techniques for dynamic voltage, temperature, and aging variation tolerance,” in Proc. Symp. VLSI Circuits, Jun. 2009, pp. 112–113.

[6] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, “A 93% efficiency reconfigurable switched-capacitor DC-

-
- DC converter using on-chip ferroelectric capacitors, in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), Feb. 2013, pp. 374–375.
- [7] M. J. Turnquist, J. Makipaa, M. Hienkari, H.-P. Le, and L. Koskinen, “Rethinking DC-DC converter design constraints for adaptable systems that target the minimum-energy point,” in Proc. IEEE Int. Symp. LowPower Electron. Design (ISLPED), Sep. 2013, pp. 383–388.
- [8] V. W.-S. Ng and S. R. Sanders, “Switched capacitor DC-DC converter: Superior where the buck converter has dominated,” Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, Berkeley, CA, USA, 2011.
- [9] M. Fojtik et al., “Bubble Razor: Eliminating timing margins in an ARM cortex-M3 processor in 45 nm CMOS using architecturally independent error detection and correction,” IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 66–81, Jan. 2013.
- [10] https://en.wikipedia.org/wiki/Multiply%E2%80%93accumulate_operation