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236 – 239

High Speed and Area Efficient Carry Skip Adder for AES Applications

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***Abstract*:** In this paper we use carry skip adder structure. This carry skip adder structure has very high speed and low power consumption.To improve the efficiency of the conventional carry skip adder (conv-CSKA) speed enhancement is taken. This speed enhancement is achieved by the providing concatenation and incrementation schemes. In this proposed structure we use AND-OR inverter (AOI) and OR-AND inverter (OAI) gates for skip logic. We use two realizations in this proposed architecture they are fixed stage size and variable stage size. This both realizations increase the speed and energy parameters of the adder. At last in the proposed structure we use a hybrid variable latencyextension which reduces the power consumption. This variable latency extension uses a modified parallel structure to increase the slack time.The proposed structure is obtained by comparing the speed, power, energy parameters. This parameter use adders with a 45-nm static technology. Now the results are obtained in HSPICE simulation with the improvement of 44% in delay and 38% in energy. In this paper we use power delay products which are very low and the proposed hybrid variable latency simulation provides reduction in power consumption and also provides speed as high.

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I. INTRODUCTION

In the arithmetic and logical unitsadders are the basic building blocks. The main purpose of the adders is to increase the speed and reduce the power consumption in the processors.Basically in general purpose processors the speed and energy consumption are highly desirable to achieve. To reduce the power consumption in digital circuits we use one of the effective techniques. This technique reduces the supply voltage that is occurred due to the switching energy. Coming to the subthreshold current, this one is the leakage component in off devices. The ON and OFF operation of the device depends on the reduction of supply voltage. If the device is ON then it resides the device into three regions. They are given as super threshold, near threshold and sub threshold regions.

Coming to super threshold region it low delay, high switching and leakage powers compared to the both near threshold and sub threshold. Next one is sub threshold region, it gives logic gate delay and leakage power. To operate circuit in sub threshold regions a small threshold current is taken for large delay.Last one is near threshold region, it provides the tradeoff between delay and power dissipation. It produces lower delay compared to sub threshold region and low switching and leakage powers compared to the super threshold region. To reduce the power consumption in this entireadder the voltage should be varied depending upon the requirement of work. To obtainhigh speed at lower supply voltages computational blocks are used.

To optimize the speed and power of different number ofadder structures and familiesare used.For example they are given as ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA) and parallel prefix adder (PPA). Let us first discuss about the carry skip adder, it is the simplest structure and occupies small area. Next one carry Select adder, the speed, area and power consumption is large compared to the RCA. Coming to the parallel prefix adder, isalso known as look ahead carry adder and it generates the carry as early as possible.

Next one is carry skip adder, in this the power consumption is very low and occupies small area. The proposed carry skip adder structure has many features like it maintains low area and low power consumption. A variable latency technique is used to reduce the power consumption. The carry skip adder works under the regions from sub threshold region to near threshold region. There are some contributions in the carry skip adder which are shown in below

1. By combining the both concatenation and incrementation schemes we can propose modified carry skip adder structure that is conventional carry skip adder. In this proposed structure the speed and energy is enhanced.
2. To construct an efficient carry skip adder structure a design strategy is provided. This strategy depends on the analytical expressions.
3. Providing impact on the efficiency of voltage scaling in the proposed carry skip adder structure.
4. At last proposing a hybrid variable latency on the proposed carry skip adder structure.

II. PROPOSED CSKA STRUCTURE

A. General Description of the Proposed Structure

The below figure (1) shows the architecture of the proposed carry skip adder. As discussed earlier that carry skip adder mainly depends upon the combination of both concatenation and incrementation schemes.

 ISSN: 2454-4248
236 – 239

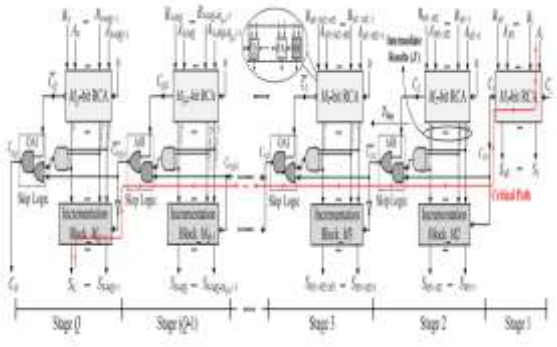

FIG. 1. PROPOSED CI-CSKA STRUCTURE

In this proposed architecture we use simple carry skip logics. The main intent of this skip logics is to replace the multiplexers by AND-OR inverter (AOI) and OR-AND inverter (OAI)compound gates. This compound gates consist of transistors, this adder provides low delay, lowpower and low power consumption. The above structure is complemented when carry propagates through the skip logics. Now at the output the carry is generated. Because of this it produces low propagation delay and occupies low area. Here the power consumption is smaller than the multiplexers.

In the internal architecture of proposed structure, the adder contains two N bits inputs, A and B, and Q stages. Each stage consists of RCA block with size of M_j. in the proposed structure all the inputs of RCA block is zero except first block. Coming to the first stage it has only one block, which is RCA. Next is stages 2Qit consist of two blocks of RCA and incrementation. The main purpose of this incrementation block is to note the intermediate results that are generated by the RCA block and carry output of the previous stage.Basically the internal structure of proposed structure consists ofchain half adders which are shown in below figure (2).

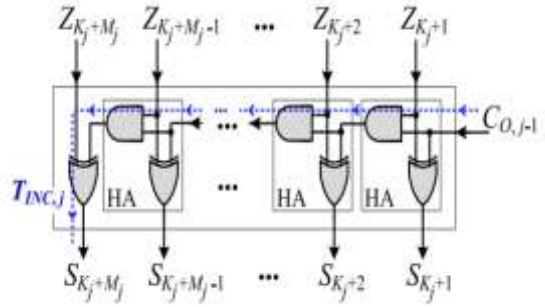

FIG. 2. INTERNAL STRUCTURE OF THE JTH INCREMENTATION BLOCK

To reduce delay we will not use carry output of incrementation block. The main purpose of using AOI and OAI gates are to invert the functions in standard cell libraries. From figure (1) we can say that if AOI is used as skip logic and for the next skip logic function is used as OAI. In the conventional carry skip adder the delay of the critical path increases. To solve this problem in the proposed structure we use the RCA block with carry input of zero.

B.Stage Sizes Consideration

Basically the conventional carry skip adder architecture is implemented by using the FSS and VSS. The stage size for RCA and incrementationblock is same.The below figure (3) shows the Sizes of the stages in the case of VSS for the proposed and conventional 32-bit CSKA structures in 45-nm static CMOS technology. In the below figure the dashed and the dotted lines shows the rate of size increases and decreases. When the size is increases and decrease is balanced then in proposed structure decreased one more than the increased one.

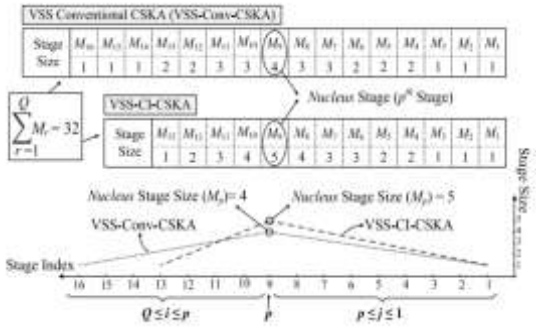

FIG. 3. SIZES OF THE STAGES IN THE CASE OF VSS FOR THE PROPOSED AND CONVENTIONAL

III. PROPOSED HYBRID VARIABLE LATENCY CSKA

Let us first discuss about the generic structure of the variable latency adder which is based on the RCA. The below figure (4) shows the generic structure of variable latency adder based on the RCA. In this the adders activate the critical paths very rarely. If the critical paths are activated then we require two clock periods to complete the operation and in the same way if the critical paths are not activated then only one clock period is enough to complete the operation.So the both longest off critical paths and longest critical paths determine the maximum amount of voltage supply scaling.

From the below figure (4) we can observe that the predictor block consists of both AND and XOR gates which determines the product of propagate signals.Finally to predict the activation of the critical path some middle bits are used. In thisthe carry propagation path from the first stage to the Nth stage is the longest critical path the carry propagation path from first stage to the (j+m)th stage and the carry propagation path from (j +1)th stage to the Nth stage is longest OFF critical paths.

ISSN: 2454-4248
236 – 239

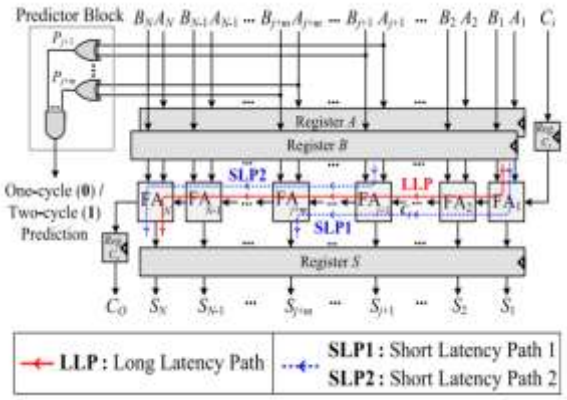

FIG. 4. GENERIC STRUCTURE OF VARIABLE LATENCY ADDERS BASED ON RCA

Upto now we have discussed about the proposed structure of carry skip adder and the generic structure of the variable latency adder.Now let us discuss about the proposed structure of hybrid variable latency carry skip adder.The below figure (5) shows the proposed structure of variable latency carry skip adder.

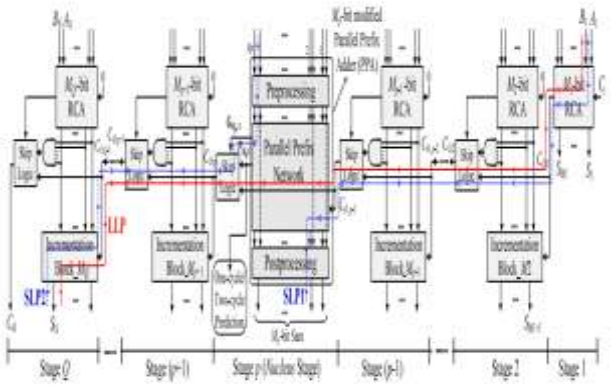

FIG. 5. STRUCTURE OF THE PROPOSED HYBRID VARIABLE LATENCY CSKA.

From the above figure (5) we can observe that for the p_{th} stagean Mp-bit modified PPA is used. In the proposed hybrid variable latency carry skip adder consists of nucleus stage. In this nucleus stage the size is very large because of this the delay will reducesthe slack time in the proposed structure increases because of the fast PPA.

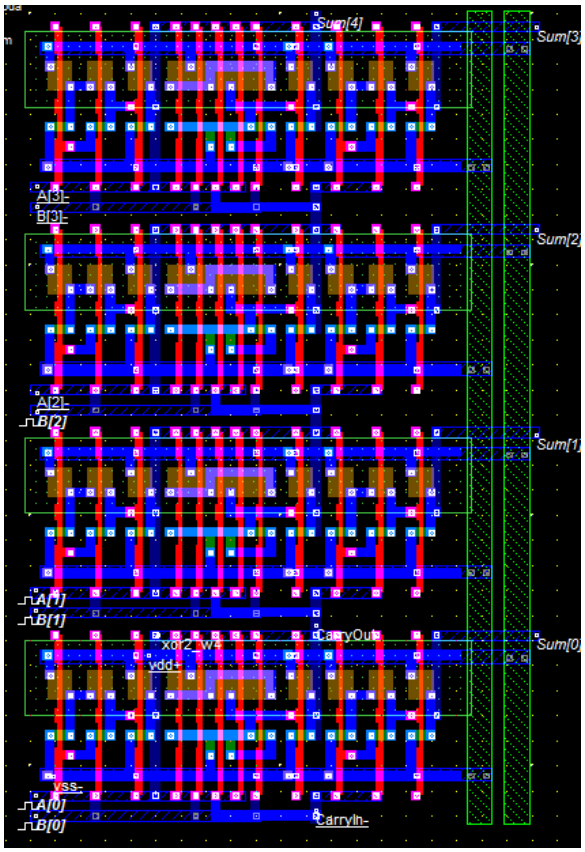

FIG. 6. SCHEMATIC

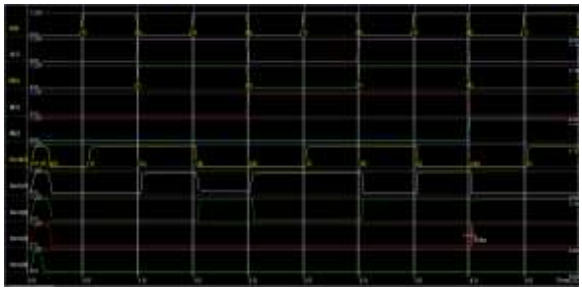

FIG. 7. OUTPUT WAVEFORM

IV. CONCLUSION

As discussed earlier that CMOS carry skip adder structure is also known as the Cl-CSKA. This proposed structure consists of high speed and low energy consumption. To modify the structure speech enhancement method is taken, this is obtained by the combination of both concatenation and incrementation techniques. For carry skip logics we use both ANDOR inverter and OR AND inverter.In The proposed structure the efficiency is obtained FSS and VSS. The range of the proposed structure is from super threshold to near threshold region. this is about the proposed structure of the conventional carry skip adder coming to the hybrid variable latency adder at middle stage the modified parallel adder structure is taken. Due to this the slack time is increases and power consumption becomes very low. This is

 ISSN: 2454-4248
236 – 239

one is mostly used in the applications of high speed low energy consumption.

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