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Design of Different Controllable Inverters using a Novel Technology Quantum Dot Cellular Automata (QCA)

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Abstract: Application of quantum-dot is a promising technology for implementing digital systems at nano-scale. Quantum-dot Cellular Automata (QCA) is a system with low power consumption and a potentially high density and regularity. Also, QCA supports the new devices with nanotechnology architecture. This technique works based on electron interactions inside quantum-dots leading to emergence of quantum features and decreasing the problem of future integrated circuits in terms of size. In this paper, we will successfully design, implement and simulate a new 2-input and 3-input XOR gate (exclusive OR gate) based on QCA with the minimum delay, area and complexities.

The state of each cell is affected in a very nonlinear way by the states of its neighbors. A line of these cells can be used to transmit binary information. We use these cells to design inverters, programmable logic gates, dedicated AND and OR gates, and non-interfering wire crossings. Complex arrays are simulated which implement the exclusive-OR function and a single-bit full adder.

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I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) is a Promising model emerging in nanotechnology. In QCA, binary data appear as loading quantum-dots within the cells. XOR gates are important circuits in QCA technique because they are expected to be used in adder and reversible gate at nano-scale. QCA is a known technology that can be a good replacement, for CMOS-based devices in nano-scale. After decades of its final growth the minimum feature in CMOS technology, is ultimately confronted with limitations. In QCA, binary data appear as loading quantum-dots within the cells. Numerous studies are reported in which QCA is able to produce devices with high density, low power consumption and very high switching speed.

We have recently proposed a scheme in which Coulomb-coupled quantum devices are connected in a cellular automata architecture.' We call such architectures quantum cellular automata (QCA).34 A QCA consists of an array of quantum-dot cells connected locally by the interactions of the electrons contained in each cell. The scheme is non-conventional in that the quantum state of each cell is used to encode binary information. The Coulomb interaction connects the state of one cell to the state of its neighbors. Thus the problems associated with small output currents and parasitic capacitances of connecting wires do not occur. "Binary wires" composed of linear arrays of cells are effective in transmitting information, coded in the cell states, from one place to another.

II. COUPLED QUANTUM CELLS

The standard cell design, shown schematically in Fig.1 (a), consists of five quantum dots located at the corners and the center of a square. The cell is occupied by a total of two electrons hopping among the five sites. Tunneling occurs between the central site and all four of the outer sites (near-neighbor tunneling) and to a lesser degree between neighboring outer sites (next-near-neighbor tunneling). It is assumed that the potential barriers between cells are high enough to completely suppress intercellular tunneling.

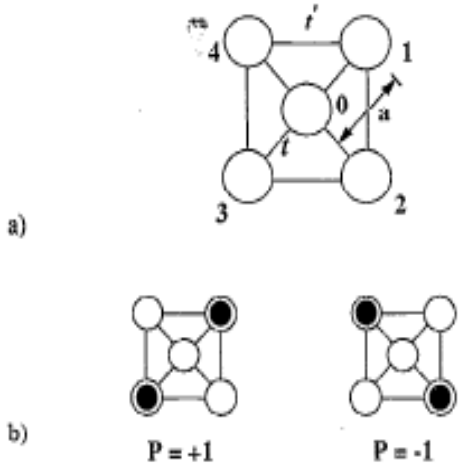

Figure 1: Schematic of the basic five-site cell. (a) The geometry of the cell.

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The tunneling energy between the middle site and an outer site is designated by t, while t' is the tunneling energy between two outer sites. (b) Columbic repulsion causes the electrons to occupy antipodal sites within the cell. These two bistable states result in cell polarizations of P= + 1and P=-1

2.1. Background

The main units of QCA are QCA cells located on the vertices of a square by four quantum-dots. There are two electrons in each cell which can be located, according to Coulomb electrostatic interaction, in diagonal position. The electrons are controlled by potential barriers and can move by tunneling and controlling the potential barriers and produce our
binary values.

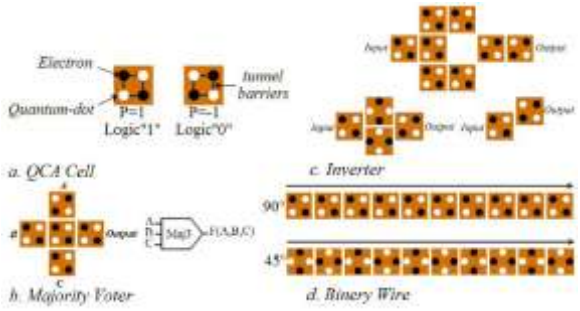

Figure 2: Basic QCA logic devices (a) QCA cell, (b) Majority voter (MV), (c) Inverter,(d) Binary wire

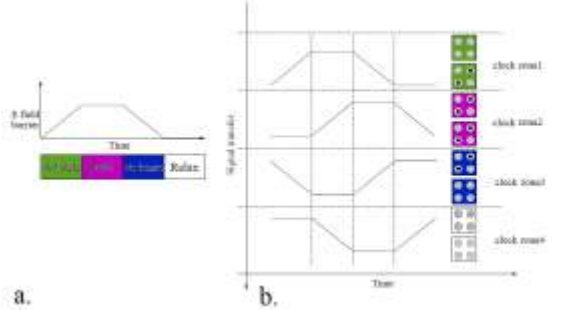

Figure 3: Four phases of the QCA clock, (b) Clock zones signal.

The electrons tend to occupy antipodal outer sites within the cell due to their mutual electrostatic repulsion as shown in Fig. 1 (b). The two stable states shown are degenerate in an isolated cell, but an electrostatic perturbation in the cell's environment (such as that caused by neighboring cells) splits the degeneracy and causes one of these configurations to become the cell ground state. Altering the perturbation causes the cell to switch between the two states in an abrupt and nonlinear manner. This very desirable bistable saturation behavior is due to a combination of quantum confinement, Columbic repulsion, and the discreteness of electronic charge.

2.2. QCA clocking

All proposed circuits in QCA not only need a clock to synchronize and control information flow but also this clock provides the necessary power to run the circuit. QCA calculations by tunneling are performed by four phases of clock signal, as you observe in Figure 2. Clocking in QCA includes four phases: hold, release, relax and switch. Each phase is 90 degrees behind the other.During switch phase, the potential barriers among quantum dots raise gradually and QCA cell will be located in one of the existing polarization states with regard to the adjacent cell. During hold phase, the barriers between quantum-dots remain at their higher levels preventing tunneling of electrons, and polarization of QCA cells will remain the same.

During release and relax phases, the barriers between quantum-dots reduce to its minimum value

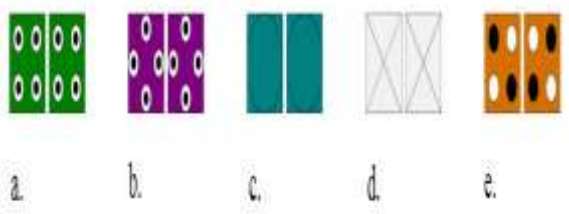

Figure 4 : QCA Designer cells: (a) normal cell, (b) rotate cell, (c) vertical cell, (d) cross over cell, (e) fix polarization cell

III. ARCHITECTURE OF PROPOSED 2-INPUT AND 3-INPUT XOR GATE IN QCA

In this article, we have designed a hierarchical circuit. First, we designed a 2-input XOR and then the 3-input XOR. With a series connection of this XOR we produced the inverter of the n-bit digits with control lines.

3.1. 2-input XOR gate in QCA

The 2-input XOR gate in the logic mode has the following function: if two input lines have the same amounts, the output value becomes "0" and if two input lines have different values, the output equals to "1". Therefore, this gate has diverse and extensive functions in different circuits. Figure 4(a) exhibits logic implementation of 2-input XOR gate and Figure 4(b) exhibits the proposed 2-input XOR

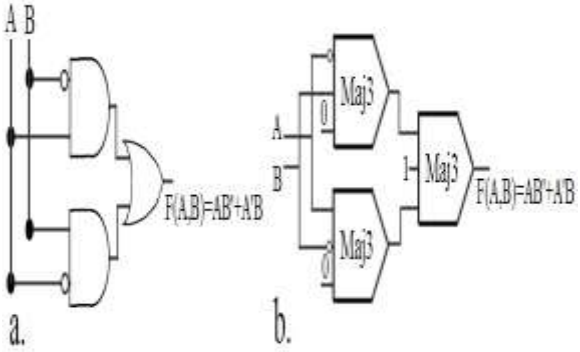

Figure 5: 2 input XOR GATE IMPLEMENTED BY (A) Logical gate (b)QCA with majority gate

This gate bears the logic equation of
F(*A***F**,**(A***B*,**)B**=**)**=*A***A**⊕**B***B*==**A'B***A*+'*B***AB**+'*AB* '

The circuit was designed and simulated for functional behavior using the QCA Designer Ver. 2.0.3. In the bistable approximation, the following parameters were used: Number of samples = 50000, Convergence tolerance = 0.001, Radius of effect = 65nm, Relative permittivity = 12.9, Clock high =9.8e-022,

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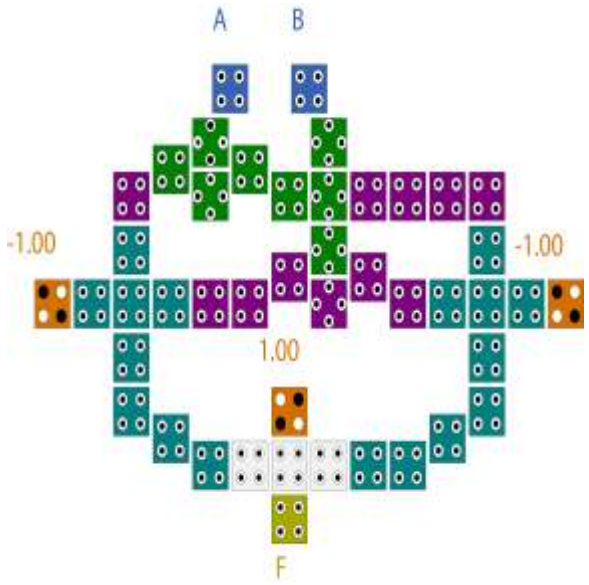

Figure 6: 2-input XOR gate implemented in QCA.

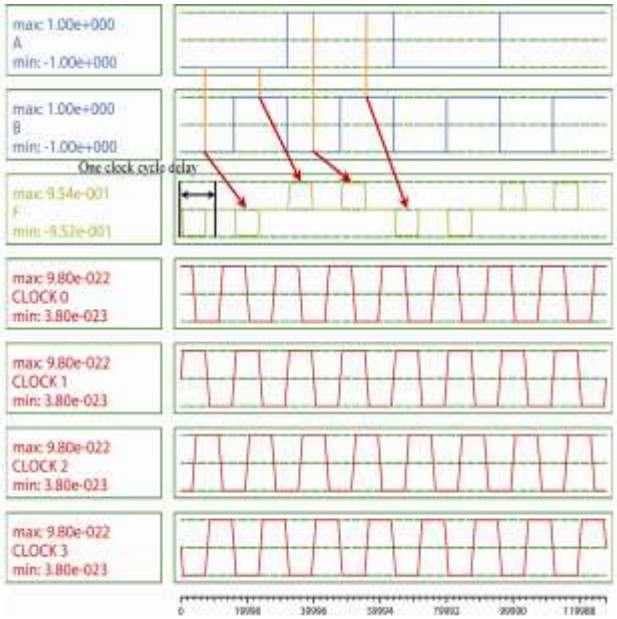

Figure 7: Simulation results for proposed 2-input XOR gate in QCA.

Clock low = 3.8e-023, Clock shift = 0, Clock amplitude factor = 2, Layer Separation=11.5, Maximum iteration per sample = 100. Implementation of 2-input XOR gate in QCA has been exhibited in Figure 5, which was implemented by the minimum cell number and complexity and reached the output in one clock cycle. The proposed 2-input XOR gate consists of 45 cells covering an area of 0.05 µm2 (278nm×178nm). The simulation results of the 2-input XOR gate is presented in Figure 6.

3.2. 3-input XOR gate in QCA

The 3-input XOR gate is a combinational circuit producing the arithmetical XOR of three bits. This circuit includes three inputs and one output. Here, we will implement our 3-input XOR using two 2-input XOR. Two input variables indicated with A and B are connected to the first-stage of XOR gate.

The third input C is lower value and connected to the second-stage of XOR gate. The 3-input XOR gate in the logic mode has the following function: if three input lines have same amounts, the output value becomes "0" and if two input lines have "0" values, the output equals "1" and if two input lines have "1" values, the output equals to "0". Therefore, this gate has diverse and extensive functions in different
circuits. Figure7(a) exhibits logic implementation of 3-input XOR gate and Figure 7(b) exhibits the proposed 3-input XOR gate implementation in QCA technique.

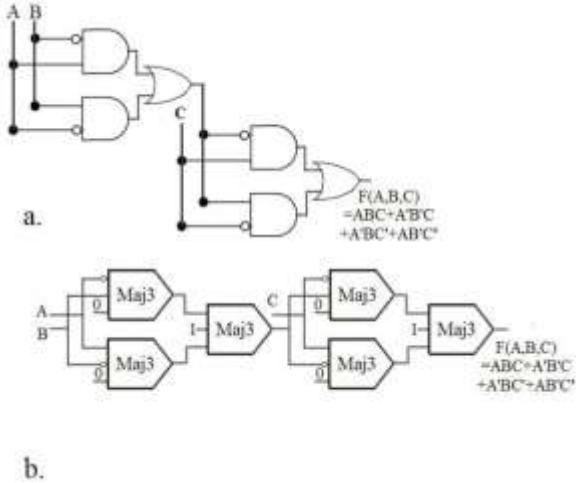

Figure 8: 3-input XOR gate implemented by (a)Logical gate (b)QCA with majority gate

This gate bears the logic equation of

$$F(A,B,C) = A \oplus B \oplus C$$
$$= ABC + A'B'C + A'BC' + AB'C'$$

And has a truth table as per Table I.

Table I: *Truth table of the 3-input exclusive OR(XOR) gate*

C	A	B	F(A,B,C)
0	0	0	
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Implementation of 3-input XOR gate in QCA is exhibited in Figure 8, which was implemented by the minimum cell number and complexity and reached the output in two clock cycles.

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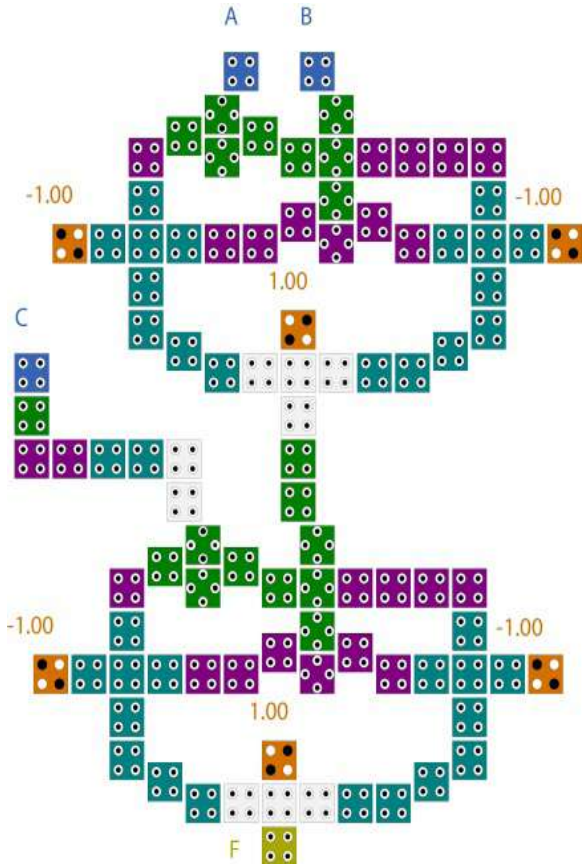


Figure 9: 3-input XOR gate implemented in QCA.

The proposed 3-input XOR gate consists of 98 cells covering an area of 0.13 μm2. The simulation results of the 3-input XOR gate is presented in Figure 10.

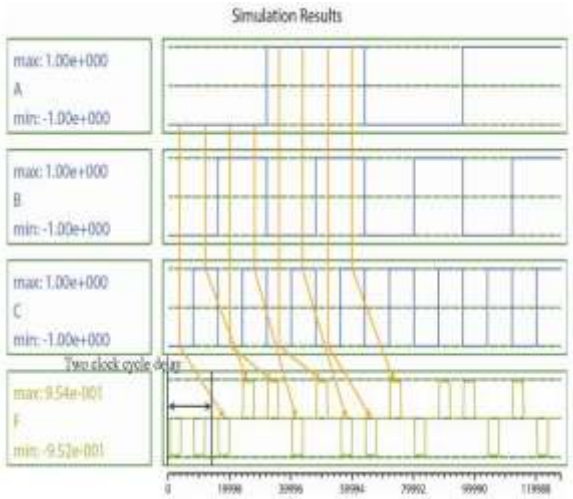


Figure 10: simulation result 3 input XOR gate

IV. CONTROLLABLE INVERTER IMPLEMENTATION IN QCA

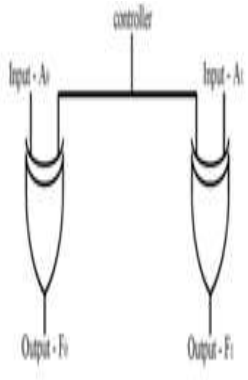
The controllable inverter is a combinational circuit which performs arithmetic operations i.e. inverted the binary digits. In this paper, we have designed a hierarchical circuit. First, we designed a controllable inverter based on 2-input XOR gate. With a series connection of two or four 2-input XOR gate, we obtained the inverted of 2 and 4-bit. Then, the controllable inverter circuit was made by 3-input XOR gate. We have designed 2 and 4-bit double controllable inverter with 3-input XOR gate in QCA.

4.1. Controllable inverter implementation with 2-input XOR gate in QCA

In order to implement controllable inverter circuit, we used the proposed 2-input XOR gates and 2-input XOR gate features in nverter operations. In the first state, two 2-input XOR gates were located next to each other. Then we connected one of the input gate pins to two input data, and other pins
were connected to each other and used as controller input. In this circuit, if the control input was loaded on zero, the output aimed the same value, and if the control input was loaded on one, the output was inverted. The layout of 2-bit controllable inverter in QCA is presented in Figure 11.
In the second state, four 2-input XOR gates were located next to each other. Then we connected one of the input gate pins to four input data, and other pins were connected to each other and used as control input. The layout of 4-bit controllable inverter in QCA is presented in Figure 12.

4.2. Double controllable inverter implementation with 2-input XOR gate in QCA

In order to implement double controllable inverter circuit, we used the proposed 3-input XOR gates and 3-input XOR gate features in inverter operations. In the first state, two 3-input XOR gates were located
next to each other. Then we connected one of the input gate pins to two input data, and twin other pins were connected to each other and used as controller input. In this circuit, if the two control input was loaded on “00 & 11”, the output remained the same value, and if the control input was loaded on “01 & 10”, the output was inverted. The layout of 2-bit double controllable inverter in QCA is presented in Figure 12. Generalizing this 2-bit double controllable inverter provided only requires a driver circuit. For example,
if we want a 4-bit double controllable nverter implementations, we need four, 3-input XOR gates. This 4-bit double
controllable inverter will attain the output in the three clock cycles.



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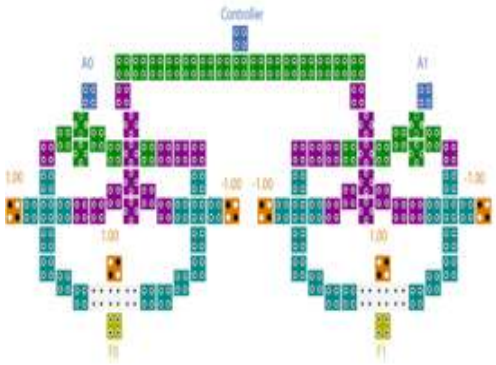

Figure 11: 2-bit controllable Inverter implemented in QCA

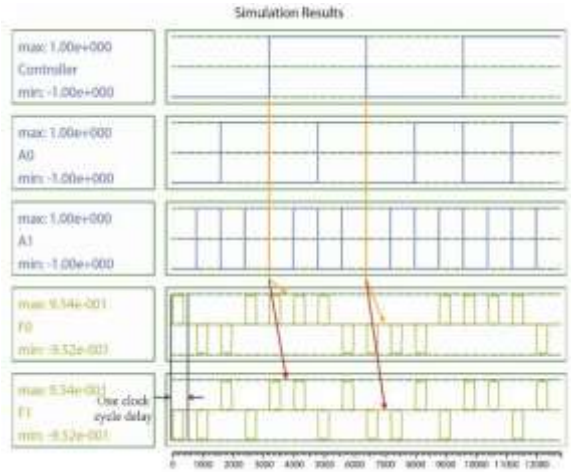

Figure 12: Simulation results for proposed 2-bit controllable inverter in QCA.

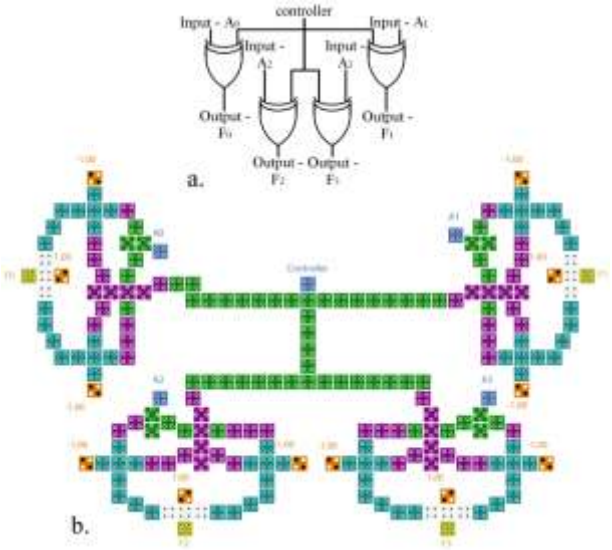

Figure 13:4 bit controllable inverter implementation in QCA

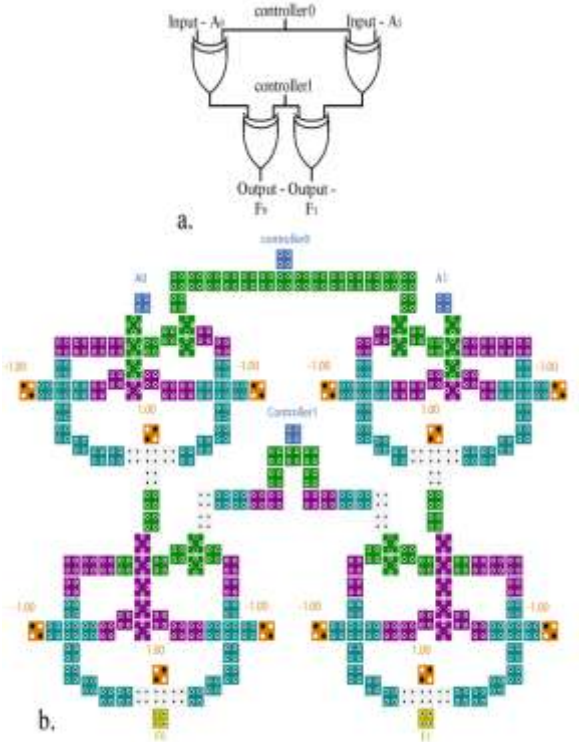

Figure 14: 2 bit double controllable inverter implemented in QCA

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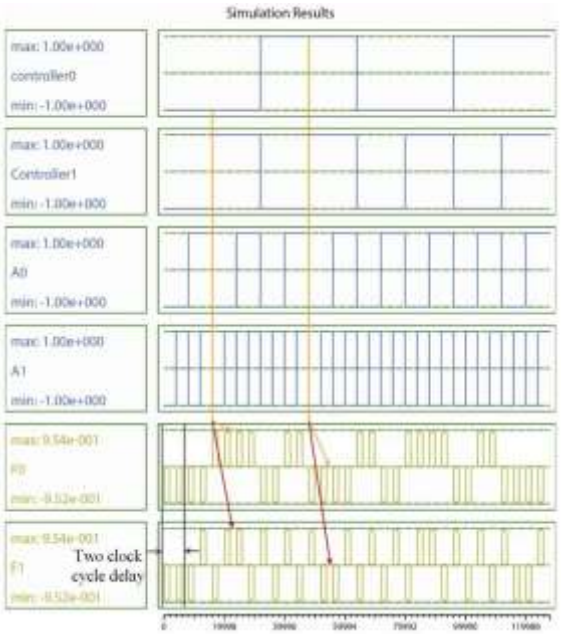

Figure 15 Simulation results for proposed 4-bit Controllable inverter in QCA

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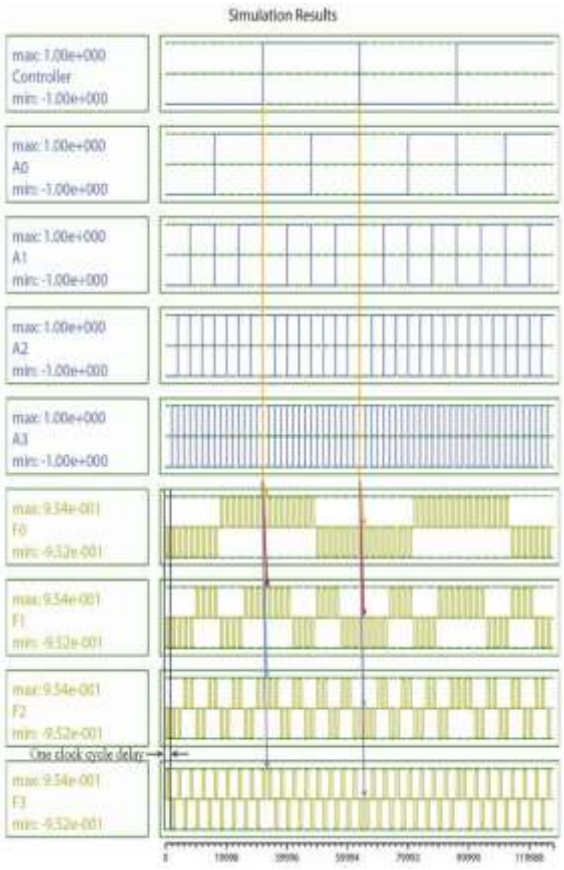

Figure: 16 simulation results for proposed 2 bit double controllable inverter

V. CONCLUSION

We have proposed a new extendable design of 2-input and 3-input XOR gate in QCA technique. Using proposed XOR gates in this paper, the 2-bit and 4-bit controllable Inverter and 2-bit double controllable inverter gates have been designed and implemented with minimum delay, complexity and area in QCA. This controllable Inverter may be used for eversible gate or adder/subtractor for implementations with inverted circuit, which considering the pipeline is of QCA, the operational speed will be high and the consumption power and the delay will be very low.

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