Study of Various High Speed and Low Power Divide-by 2/3 Prescalers

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Abstract: Mobile gadgets plays an important role in daily life. For this low power processes are major concern. As the battery life time is limited by the power consumption which leads to more stable performance of device. Different types of ÷ 2/3 prescalerare reviewed and compared on the bases of logic style used in designing. ÷ 2/3 prescaler plays an important role in frequency synthesizer. In modern flexible frequency synthesizers prescalers should satisfy two opposing requirements low power and high speed. TSPC based ÷ 2/3 dual modulus prescaler consumes less power as compared to MCMLs at the cost of low operating speed. The ETSPC cells helps to reduce number of stacking transistors by one, which leads to increase in speed but at the same time increase power consumption of design and use of implication logic with merging techniques leads to give efficient ÷ 2/3 prescaler in terms of power consumption and operating speed.

Keywords: *MOS current mode logic(MCML), True-single-phase-clock (TSPC), Extended-true-single-phase-clock ETSPC, Flip-Fops, prescaler, implication logic, negation IMP.*

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I. INTRODUCTION

Presentdays, versatile remote communication assumes a vital job in day to day life. For this low power tasks are real worry for the portable units as the battery life time is restricted by the power utilization and this additionally results in progressively stable execution of gadget. In present day transreceiverarchicture, a completely incorporated frequency synthesizer with low power phase lock loop (PLL) and prescalers is a subject of interest for research.One of the basic utilitarian block in frequency synthesizers is the dual modulus prescaler.Prescaler is an electronic circuit which divides the high input frequency into lower output frequency.Division ratio is N or N+1 according to fedded control signal to avoid the generation of narrowly spaced frequencies at the output[2].It can work athigher frequencies and have more control than some other circuit blocks of the frequency synthesizer.Thus, the structure of dual modulus prescaler is so important. A dual modulus prescaler for the most part comprises of a divide by-2/3 prescaler unit followed by a few divide by-2 units[1]. These divide by 2/3 dual prescalers are implemented using flip-flops and higher operating frequency is determined by these flip-flops.The correct assurance of flip-flops is particularly essential which is done dependent on variables like low power, transistor count, clock load, structure strength, control delay, and power-region trade-offs are all things considered well-completely considered before picking an explicit flip-flop structure. Master slave flip-flops are all around utilized for low power systems however other flip-flops like pulse triggered flip-flops finds their usage in fast applications [2], [3].

Topologies like current-mode logic (CML), true single-phase clocked (TSPC) logic, and extended TSPC (ETSPC) logic are available to operate prescalers in GHz range.

In this paper comparison betweenthese topologies based ÷ 2/3 prescaler has been done on the bases of operating frequency, transistor count, power consumption, power delay product (PDP) and delay.

II. MCML BASED DIVIDE (÷) BY 2/3 PRESCALER

It is hard to plan a fast CMOS circuit working close of the MOS gadget. CMOS logic-based circuits are acknowledged at the cost of a static power consumption, which must be kept as little however much as could reasonably be expected. An attractive methodology as far as circuit works at higher frequency, bring down power consumption, high information exchange and high immunity to noise is MCML. MCML utilizes differential logic circuit for transmission of information. Transmission of information is done in mass at once. Transmission is point to point and unidirectional. By utilizing differential logic MCML have favourable circumstances of differential logicstyle [15].

Mostly first stage of frequency synthesizer and phase lock loop (PLL) i.e. ÷2/3 and ÷4/5 prescaler are implemented using MCML logic [17]. Dividers implemented using MCML operates at higher frequency but at the cost of high-power dissipation and provide higher immunity to noise [16].

III. ETSPC BASED÷2/3 PRESCALER

In this section ETSPC based divide by 2/3 prescalers are discussed.In ETSPC logic there is one stacked transistorless into each branch of TSPC logic. It is improved version of TSPC logic. Due to reduced number or transistor there is less switching stage as a result this logic style. Use of this logic style is to design circuits which works at high operating speed but at a cost of more short circuit path its

also leads to more power consumption as compared to TSPC logic style.

In ETSPC based ÷2/3 unit in [4] when the modulus control MC is reliably high, the output of D Flip-Flop(DFF)1 will be ceased to achieve the ÷2 work. Right when MC is set to low, it plays out the ÷3 work. Regardless, both DFFs work paying little respect to whether DFF1 doesn't increase the ouput in ÷2 mode. The restriction of this circuit is that the power dissipation because of short circuit path is more since the load capacitance is large, the operating frequency is constrained and having long critical path [4].

From the ETSPC based ÷2/3 designin [5] the yield of DFF1 will be blockedto achieve the ÷2 operation, when the modulus control (MC) is reliably high. At the pointwhen MC is low, it works in as the ÷3 mode. At the point when MC=0 in ÷2 mode, due to missing of short circuit path in the second and third period of DFF1 and hence the power utilization is reduced. This design is better than design in paper 4 since critical path is missing and therefore eat up less power [5].

Power consumption in design of [6] is high due to short circuit path between two d flip-flops and number of transistors is also more [6].

÷2/3 prescalerin [9] is implemented using improved ETSPC (IETSPC) logic which overcomes the drawbacks of both TSPC and ETSPC i.e. low speed and high-power consumption respectively. It has high operating frequency and optimum power consumption as compaired to existing prescalers. In ÷ 2/3 prescaler design of this paper, transistor count is fewer thus power dissipation and delay are alsofewer as compare to design in [4]and [5].

IV. TSPC BASED ÷2/3 PRESCALER

True Single-Phase Clocks (TSPC) have to be used to reduce the circuit complexity, power dissipation and increase the operation speed.TSPC logic have latches controlled by single phase clock in their logic gates [18]. On cascading three inverter stages of TSPC in [18] one can implement efficient 7 different DFF.

The ÷ 2/3 dual modulus prescaler using TSPC logic presented in [11]. In this design TSPC logic style is used for implementation of DFFs and logic gate (NOR) are merged into DFFs.When MC=0 and CLK=1(positive edge), transistor M0 is ON and transistor M1 is OFF. Consequently, node S1 pulled up to 1(Vdd) and node pulled down to 0 (Gnd). Transistor M5 turns OFF and M3 remains ON. The ÷ 2/3 dual modulus prescaler works similar to the TSPC DFF divide by 2 dividers. After divide by 2 operation at falling edge of signal CLK the output signal Qn2 and T1 is low, node S2 turns from low to high and node S2 and T2 remains at high (1) during whole negative cycle of clock signal CLK. At again rising edge of the CLK, node T2 is pulled down to 0. Output Qn2 turns from low (0) to high(1), node S1 and S2 is pulled down to 0. On the other hand, node T1 is pulled up. Thus, at MC=1 designed circuit will work in divide by 3 operation.

÷ 2/3 dual modulus prescaler in [11] using TSPC logic is simulated in 180-nm CMOS process where 1.5 V is supply voltage. 8.8 GHz is the highest operating frequency ofabove circuit [11].

The ÷ 2/3 dual modulus prescaler using TSPC logic in [11] is implemented using of DFFs (DFF1 and DFF2) and logic gate (AND & OR) are merged into DFFs. When MC=0, this prescaler works in divide by 3 mode. Once, when the output of DFF1 is high it precharge the node P2 and DFF2 is delayed by one clock cycle which leads to extend the division ratio to 3. When MC=1, this prescaler works in divide by 2 mode (DFF1 will work similar as of the TSPC DFF divide by two mode). The first two branches of DFFs are same and shows same switching activity when MC=0. First branch of DFF1 (consist transistor M2, M4, M5) and first branch of DFF2 (consist of transistor M12, M13, M14) can be merged together by absorbing transistor M1 and M3 (these are for module control) in the middle branch of DFF1. In improved prescaler transistor M7 is added in the precharge branch in series with the transistor to create a NOR gate at the DFF2 input. Transistor M5 is added in series with middle branch of DFF1to module control logic. This transistor creates a AND gate logic at DFF1 input.When MC=0, thisprescaler works in divide by 2 mode as the output of DFF1 is tied to a low voltage.

This prescaler is carried out in a standard 65nm CMOS process where 1.2 V is supply voltage at 290K. Maximum operating frequency is achieved is 28.5 GHz in divide by 3 mode [12].

The prescaler in [13] the NOR gate is merged into the third stage of DFF1 using transistor M10, where its drain is connected to node S3. Other NOR gate is embedded into first stage of DFF2.

This prescaler is simulated in 180nm CMOS process with 1.8 V supply voltage. The maximum operating frequency of prescaler is 5.5GHz and maximum power consumed is 0.69mV at divide by 3 mode [13].

The basic ÷ by 2/3 dual modulus prescaler includes two DFF and two logic gates (NAND and NOR). Use of logic gates limits the performance of the prescaler but also provide a maximum satisfying speed of operation at the cost of larger power consumption in design. The prescaler in [14] is implemented using TSPC logic. Here, circuit is modified by using implication logic (IMP) and negation IMP (NIMP). This circuit is more efficient than logic gate-based circuit When MC=1, the prescaler works at divide by 3 mode. the node T1 is pulled down to 0 when output of

DFF1 Qn2 stays at logic high and extend the output period by one clock cycle.When MC=0, the prescaler works at divide by 2 mode. Here, output of DFF1 is fixed to low and the last two branches static which makes the prescaler operates like a TSPC DFF.

This prescaler is simulated in 130nm CMOS process with 1.3 V supply voltage. The maximum operating frequency of prescaler is 14.1GHz and maximum power consumed is 1.2mV at divide by 3 mode[14].

Divide by 2/3 prescaler in [14] gives a perfect balance between power consumption, operating speed and transistor count.

V. CONCLUSION

TSPC based ÷ 2/3 dual modulus prescaler consumes less power as compared to CMLs at the cost of low operating speed. The ETSPC cells helps to reduce number of stacking transistors by one, which leads to increase in speed but at the same time increase power consumption of design. Here, we explore a new era of implication logic by which we can reduce the transistor count and increase the operating speed in a moderate manner. And also, by using merging techniques explored above one can easily modify the circuit implemented using implication logic. IETSPC topology is also an area of interest in terms to at operating frequency designs.

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